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**Parameters of thyristor-based surge protective
devices for the protection of telecommunication
installations**

Recommendation ITU-T K.28



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Parameters of thyristor-based surge protective devices for the protection of telecommunication installations

Summary

Recommendation ITU-T K.28 defines the parameters, test circuits and performance values of thyristor-based surge protective devices (SPDs) used for the protection of telecommunication installations (for example, exchange equipment, access equipment, telecommunication lines and subscriber or customer equipment).

This Recommendation should be used for the harmonization of existing or future specifications issued by thyristor-based SPD manufacturers, telecommunication equipment manufacturers, administrations or network operators.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T K.28	1991-03-18	V
2.0	ITU-T K.28	1993-03-12	V
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Keywords

In-line SPD, leakage resistance, overvoltage protector, surge protective device, SPD, thyristor.

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Table of Contents

	Page
1 Scope	1
2 References.....	2
3 Definitions	2
3.1 Terms defined elsewhere.....	2
3.2 Terms defined in this Recommendation.....	3
4 Abbreviations and acronyms	4
5 Conventions	4
6 Electrical parameters	5
6.1 Overvoltage function characteristics	5
6.2 Series element characteristics.....	7
6.3 Signal characteristics	9
6.4 Ratings.....	10
6.5 Overload parameters.....	12
7 Test methods.....	13
7.1 Characteristics	13
7.2 Series element characteristics.....	16
7.3 Signal characteristics	18
7.4 Rating tests	19
7.5 Overload parameters.....	20
8 Identification.....	21
8.1 Marking	21
8.2 Documentation	21
9 Ordering information.....	21
Annex A – Impulse generators.....	22
A.1 Introduction	22
A.2 Waveform tolerances.....	22
A.3 1.2/50 – 8/20 impulse generator	23
A.4 10/700 impulse generator	23
A.5 10/1000 impulse generator	23
A.6 8/20 current impulse generator.....	23
Bibliography.....	24

Introduction

Thyristor overvoltage protectors are often likened to the solid-state equivalent of gaseous discharge overvoltage protectors like the gas discharge tube (GDT) [b-ITU-T K.12]. While the general protection principles of thyristors and GDTs are similar, the test circuits for parametric measurement are often not the same due to technology differences. Thyristors require significant current to transition from a voltage limiting condition into low-voltage conduction and have a lower inherent surge current capability. Thyristor overvoltage protectors are used in environments where the surge levels are known and a well-defined voltage limiting level is needed.

Recommendation ITU-T K.28

Parameters of thyristor-based surge protective devices for the protection of telecommunication installations

1 Scope

This Recommendation applies to thyristor-based surge protective devices (SPDs) to be used for primary protection against surges due to lightning or power disturbances on telecommunication circuits, in accordance with [b-ITU-T K.11]. It covers the following device parameters:

- a) Characteristics
 - 1. Overvoltage function
 - i. Impulse limiting voltage
 - ii. Leakage current and insulation resistance
 - iii. Holding current
 - 2. Series element
 - i. Hold current
 - ii. Trip current
 - iii. Time-to-trip
 - iv. Impulse let-through current
 - 3. Signal
 - i. Capacitance
 - ii. Longitudinal conversion loss (LCL)
 - iii. Insertion loss
 - iv. Return loss
- b) Ratings
 - 1. Rated peak impulse current
 - 2. Impulse durability
 - 3. AC durability
- c) Overload parameters
 - 1. High impulse current
 - 2. Power fault
- d) Identification and marking.

This Recommendation does not deal with:

- a) mountings for SPDs and their effect on arrester characteristics;
- b) hybrid SPDs where the thyristor voltage limiting is augmented by other technologies;
- c) mechanical dimensions;
- d) quality assurance requirements;
- e) units containing heat-coils.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

- [ITU-T K.20] Recommendation ITU-T K.20 (2011), *Resistibility of telecommunication equipment installed in a telecommunications centre to overvoltages and overcurrents*.
- [ITU-T K.21] Recommendation ITU-T K.21 (2011), *Resistibility of telecommunication equipment installed in customer premises to overvoltages and overcurrents*.
- [ITU-T K.45] Recommendation ITU-T K.45 (2011), *Resistibility of telecommunication equipment installed in the access and trunk networks to overvoltages and overcurrents*.
- [ITU-T K.82] Recommendation ITU-T K.82 (2010), *Characteristics and ratings of solid-state, self-restoring overcurrent protectors for the protection of telecommunications installations*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 electronic current limiter (ECL) [ITU-T K.82]: A device based on transistor and related technology that automatically restricts the current amplitude when it exceeds a predetermined threshold level.

3.1.2 fault current, I_{fault} [b-IEC 62319-1]: Current used when measuring time-to-trip.

3.1.3 hold current (self-restoring overcurrent limiter), I_{H} [ITU-T K.82]: Maximum current at specified ambient temperature, which will not cause the trip event.

NOTE – Sometimes known as rated or non-tripping current.

3.1.4 holding current (thyristor overvoltage limiter), I_{h} [b-IEC 61643-341]: Minimum anode, principal, or thyristor current that maintains the thyristor in the on-state.

NOTE – The holding current test is the thyristor equivalent of the holdover test of a gas discharge tube.

3.1.5 impulse generator charge voltage, V_{C} [ITU-T K.82]: Value of impulse generator charging voltage.

3.1.6 insertion loss (of a two-port device) [b-IEV 702-07-08]: The ratio, generally expressed in decibels, of the apparent power at a point in a transmission channel to the power at the same point after insertion of a given two-port device into the transmission channel immediately ahead of this point.

NOTE – If the ratio defining the insertion loss is less than one, its decibel value is negative, and its converse or opposite decibel value called "insertion gain" may be used.

3.1.7 longitudinal conversion loss (LCL) [b-CISPR 16-1-2]: In a one- or two-port network, a measure (a ratio expressed in dB) of the degree of unwanted transverse (symmetric mode) signal produced at the terminals of the network due to the presence of a longitudinal (asymmetric mode) signal on the connecting leads.

3.1.8 port [b-IEV 131-12-60]: Access to a device or network where electromagnetic energy or signals may be supplied or received or where the device or network variables may be observed or measured.

NOTE – An example of a port is a terminal pair.

3.1.9 reflection loss factor [b-IEV 131-12-65]: Ratio of the apparent power that a specified source would deliver to a load with zero reflection factor at its interface with the source, to the apparent power delivered by the same source to a directly connected given load.

3.1.10 return loss [b-IEV 702-07-25]: The modulus of the reciprocal of the reflection factor, generally expressed in decibels.

NOTE – When impedances can be defined, the return loss is given by the formula:

$$-20\lg(r) = 20 \left| \frac{(Z - Z')}{(Z + Z')} \right|$$

where Z is the characteristic impedance of a transmission line ahead of a discontinuity, or the impedance of a source, and Z' is the impedance after the discontinuity or the load impedance seen from the junction between the source and the load.

3.1.11 surge protective device (SPD) [b-ITU-T K.72]: Device that restricts the voltage of a designated port or ports, caused by a surge, when it exceeds a predetermined level.

NOTE 1 – Secondary functions may be incorporated, such as a current-limiting device to restrict a terminal current.

NOTE 2 – Typically, the protective circuit has at least one non-linear voltage-limiting surge protective component.

NOTE 3 – An SPD is a combination of a protection circuit and holder.

3.1.12 time-to-trip (PTC thermistor) t_{trip} [ITU-T K.82]: Under specified ambient conditions, starting from the time the fault current (I_{fault}) is applied, the time-to-trip is the time required for a device to transition into a tripped state.

NOTE – An overcurrent protector shall have passed into the tripped condition as indicated by the measured voltage exceeding 90% of the supply open-circuit voltage.

3.1.13 trip current (self-restoring overcurrent limiter), I_t [ITU-T K.82]: Lowest current which will cause a trip event at a specified temperature and within a time specified in the product specification.

3.1.14 trip event (self-restoring overcurrent limiter) [ITU-T K.82]: Event of rapid increasing resistance in response to an overcurrent surge.

3.1.15 two-port [b-IEV 131-12-65]: Device or network with two separate ports.

3.1.16 user agreed values [ITU-T K.82]: Test parameters and circuits agreed between major stakeholders (e.g., user and manufacturer) for a specific application.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 impulse limiting voltage, V_P : Highest value of voltage across the terminals of the SPD during the application of a specified impulse.

NOTE – Also called voltage protection level or measured limiting voltage.

3.2.2 in-line SPD: A two-port SPD connected in series with the service feed.

3.2.3 insulation resistance (effective): Quotient of the voltage applied to a designated terminal pair, V_{IR} , by the current, I_{IR} , drawn from the applied voltage.

3.2.4 let-through current: In-line SPD peak short-circuit output current when a specified impulse is applied to the SPD input.

3.2.5 rated peak impulse current: Maximum value of peak impulse current of specified amplitude and waveshape that may be applied without causing degradation.

3.2.6 semiconductor arrester assembly (SAA): A surge protective device (SPD) that uses thyristor technology as the main overvoltage limiting element.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AC	Alternating Current
ADSL	Asymmetric Digital Subscriber Line
CMI	Common Mode Injector
DC	Direct Current
DSL	Digital Subscriber Line
ECL	Electronic Current Limiter
GDT	Gas Discharge Tube
LBB	Longitudinal Balanced Bridge
LCL	Longitudinal Conversion Loss
POTS	Plain Old Telephone Service
PTC	Positive Temperature Coefficient
PVC	Polyvinyl Chloride
SAA	Semiconductor Arrester Assembly
SPD	Surge Protective Device
VDSL	Very high speed Digital Subscriber Line

5 Conventions

The original version of ITU-T K.28 [b-ITU-T K.28] mainly used material from the United States of America standards available at that time. The definition of a semiconductor arrester assembly (SAA) was intended to denote a surge protective device (SPD) that used thyristor technology as the main overvoltage limiting element. Unfortunately, the term "semiconductor" covers a large range of voltage limiting components other than just a thyristor component. For this reason this version of ITU-T K.28 uses thyristor-based SPD (or simply SPD for brevity) rather than SAA.

For the protection of twisted pair cables an SPD can be connected in shunt (Figure 1-a) or in-line (Figure 1-b) with the cable. Shunt SPDs can be tested in the in-line SPD test circuits by shorting the corresponding port input and output terminals together. In-line SPDs can incorporate series overcurrent protectors, either temperature or current operated (Figure 1-c). Additional tests are required to measure the overcurrent protection element operation, surge withstand and surge current let through.

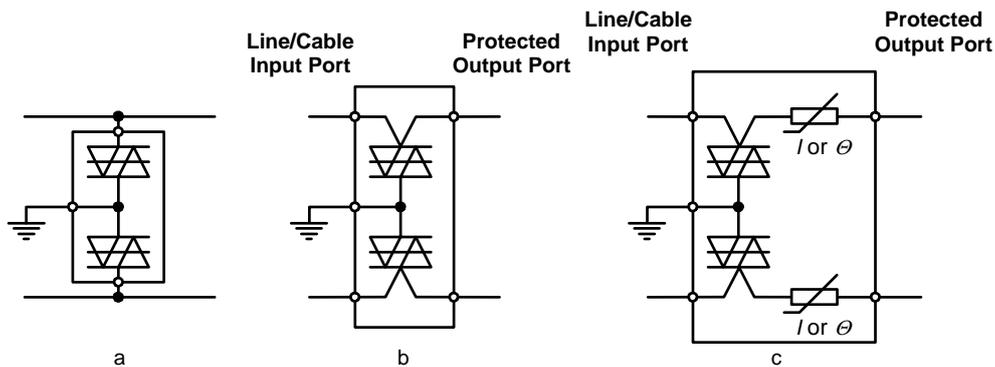


Figure 1 – SPD configuration examples

6 Electrical parameters

6.1 Overvoltage function characteristics

6.1.1 Impulse limiting voltage (Protection voltage), V_P

This parameter is the highest level of residual voltage the protected equipment is exposed to when a specified impulse is applied to the SPD.

6.1.1.1 Values

The impulse limiting voltage tends to increase at fast rates of rise. Two values of limiting voltage are measured: one under the rated impulse conditions and the other with a fast rising impulse. The values are measured in transverse and longitudinal modes for both impulse polarities.

The test method is given in clause 7.1.1.

6.1.1.2 Criteria

The measured SPD voltage limiting values, V_p , must not be greater than the product documentation, user agreed or Table 1 values.

6.1.2 Leakage current, I_{IR}

The leakage current value of a thyristor-based SPD tends to be independent of voltage up to V_{IR} . The applied test voltage value, V_{IR} , represents the maximum system voltage that can occur without clipping (see Table 1).

6.1.2.1 Values

For thyristor-based SPD, a maximum leakage current of 1 μ A at 25°C is a realistic value. Thyristor junction leakage current roughly doubles for every 10°C temperature rise.

The test method is given in clause 7.1.2.

6.1.2.2 Criteria

The measured leakage current must not exceed the product documentation, user agreed or Table 2 value.

6.1.3 Insulation resistance

The value of insulation resistance is calculated from the applied test voltage and the measured leakage current, V_{IR}/I_{IR} . The value is calculated from the results of clause 6.1.2.

6.1.3.1 Values

The preferred values of minimum insulation resistance are given in Table 1.

6.1.3.2 Criteria

The calculated insulation resistance must not exceed the product documentation, user agreed or Table 2 value.

Table 1 – Preferred leakage current, insulation resistance and voltage limiting values

Insulation resistance			Impulse limiting voltage, V_P ^{d)}	
Terminal pair applied voltage ^{e)} , V_{IR} (V)	Insulation resistance ^{e)} V_{IR}/I_{IR} (M Ω)		Voltage under rated impulse conditions ^{a), e)} (V)	Voltage under fast impulse conditions ^{b), e)} (V)
	Basic leakage level $I_{IR} < 5 \mu A$	Enhanced leakage level $I_{IR} < 1 \mu A$		
± 65	>13	>65	<90	<100
± 200	>40	>200	<265	<280
± 265	>53	>265	<340	<355
± 300	>60	>300	<400	<420
± 400	>80	>400	<550	<580
$V^{c)}$	$W^{c)}$	$X^{c)}$	$Y^{c)}$	$Z^{c)}$
<p>a) For rated impulse values, see clauses 7.1.1.1 and 7.1.1.2.</p> <p>b) For fast impulse values, see clauses 7.1.1.3 and 7.1.1.4.</p> <p>c) Product documentation values or user agreed values.</p> <p>d) The maximum voltage limiting may be set by either equipment protection requirements (e.g., [ITU-T K.21] or [ITU-T K.20] or [ITU-T K.45]), or by technology capability. Values shown are typical.</p> <p>e) The transverse voltage values can be lower if an additional voltage limiting element is connected between two input terminals. These voltage and insulation resistance values should be specified in the product documentation or be the user agreed values.</p>				

6.1.4 Holding current, I_h

The holding current, I_h , is the minimum current that maintains a switched SPD in the low-voltage on-state.

6.1.4.1 Values

Table 2 lists various values of holding current. Common values for I_h are: 150 mA and 250 mA measured at 25°C. The Table 2 bias voltage and resistance values are commonly used. As thyristors do not have a glow region restriction like gas discharge tubes, the upper limit of bias voltage becomes V_{IR} with a corresponding change in current limit resistance. The SPD holding current decreases with temperature, typically 65% of 25°C value at 70°C. If high ambient temperatures are expected, then the holding current test should be done at the highest expected ambient temperature.

The test method is given in clause 7.1.3.

6.1.4.2 Criteria

The holding current must not be less than the product documentation, user agreed or Table 2 value at the specified ambient temperature.

Table 2 – Holding current test circuit values

Holding current, I_h (mA)	Bias voltage V_{BAT}^{a)} (V)	Current limit resistance value, R (Ω)
150 @ 25°C	52	330
250 ^{b)}	52 ^{b)}	200 ^{b)}
235 ^{b)}	80 ^{b)}	330 ^{b)}
100 ^{b)}	135 ^{b)}	1300 ^{b)}
X ^{c)}	–	–
^{a)} The value of V_{BAT} cannot be $> V_{IR}$ to void possible clamping action. ^{b)} Values from [b-ITU-T K.12]. ^{c)} Product documentation value or user agreed value.		

6.2 Series element characteristics

The test approaches used in this clause are based on [ITU-T K.82], but with modifications to avoid premature activation of the SPD overvoltage protection element.

6.2.1 Hold current, I_H

This parameter defines the maximum current, which will not cause the trip event at specified ambient temperature.

6.2.1.1 Values

For compatibility, the hold current should not be less than the selected value of thyristor holding current given in Table 1. The lowest value of hold current occurs at the highest ambient temperature (see [ITU-T K.82]).

The test method is given in clause 7.2.1.

6.2.1.2 Criteria

The in-line SPD, when conducting the specified I_H current at a specified temperature, shall not have tripped during the specified measurement time. This verifies that the tested SPD I_H is higher than the specified I_H value.

6.2.2 Trip current, I_t

This parameter defines the lowest current which will cause a trip event at a specified temperature and within a time specified in the product specification.

6.2.2.1 Values

The trip current will be either specified in the product documentation values or user agreed values or twice the selected Table 1 holding current value. Normally, the trip current value will be approximately twice the hold current value, $I_t = 2I_H$. The lowest value of trip current occurs at the highest ambient temperature (see [ITU-T K.82]).

The test method is given in clause 7.2.2.

6.2.2.2 Criteria

The in-line SPD, when conducting the specified I_t current at a specified temperature, shall have tripped during the specified measurement time. This verifies that the tested SPD I_t is lower than the maximum trip current.

6.2.3 Time-to-trip, $t_{\text{trip}} @ I_{\text{fault}}$

The parameter defines the time taken from the start of the current flow for the self-restoring current limiter to transition into a tripped state. This is only applied to positive temperature coefficient (PTC) thermistor self-restoring current limiters. Due to the operating speed and mode, this test is not applied to SPDs with electronic current limiter (ECL) self-restoring current limiters (see [ITU-T K.82]).

6.2.3.1 Values

The required time to trip is often set by safety considerations. Figure 2 shows the time-current values for no damage to a 0.4 mm diameter polyvinyl chloride (PVC) covered copper wire. This type of wire is often used for internal telecommunication cables. Used with this wire, the self-restoring overcurrent protector time to trip curve should be under the wire curve of Figure 2. For example, the withstand time of the wire is 12 s at a current of 10 A, meaning that the 10 A, I_{fault} , time to trip should be less than 12 s.

The test method is given in clause 7.2.3.

6.2.3.2 Criteria

The measured time-to-trip value at a specified I_{fault} current shall be less than or equal to the specified value(s) given in either the product documentation, the user agreed values or Figure 2.

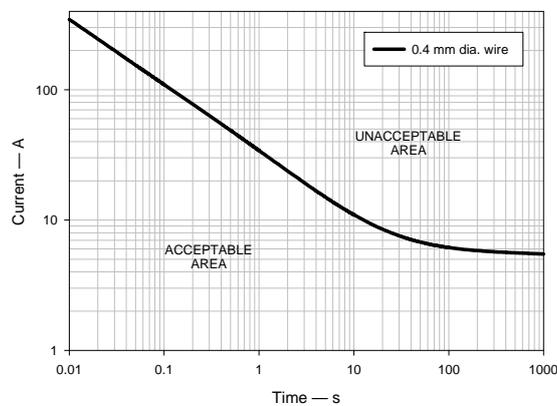


Figure 2 – Maximum current without 0.4 mm wire damage

6.2.4 Impulse let-through current

In-line SPDs with self-restoring current limiters will output a certain level of peak short current before the voltage limiter operates; this is the SPD impulse let-through current. This test does not apply to ECL series elements (see [ITU-T K.82]). Ceramic PTC thermistors have a significant resistance reduction under high voltage conditions.

6.2.4.1 Values

This parameter is measured under 10/700 μs generator impulse conditions. The typical positive temperature coefficient (PTC) thermistor resistance range used is 2 Ω to 10 Ω . The peak let-through current will depend on the effective impulse resistance of the PTC thermistor (see [ITU-T K.82]), and the SPD voltage limiting value. For example, an in-line SPD with 200 V limiting voltage value and an effective impulse series resistance of 5 ohms would have a peak let-through current of 40 A.

The test method is given in clause 7.2.4.

6.2.4.2 Criteria

The measured impulse let-through current value shall be less than or equal to the specified value given in either the product documentation or the user agreed value.

6.3 Signal characteristics

6.3.1 Capacitance

Because thyristors have multiple PN junctions, the thyristor capacitance will vary with applied voltage. This voltage variable capacitance can distort digital subscriber line (DSL) signals and reduce data rate. Various manufacturing and circuit techniques are used to reduce the capacitance variation.

6.3.1.1 Values

The capacitance between terminal and earth should not exceed the Table 3 values when tested according to clause 7.3.1. Measuring at 0 V usually gives the highest value of capacitance and no matter what the applied voltage, the total capacitance variation cannot exceed the 0 V DC value.

As it is the capacitance variation that is important, it is also permissible to measure the capacitance value at bias values of $-V_{IR}$, 0 and $+V_{IR}$. The total change in capacitance must be less than the Table 2 values. In addition the $-V_{IR}$ and $+V_{IR}$ capacitance values must be matched within 5%.

6.3.1.2 Criteria

The measured capacitance value or change in capacitance must not exceed the product documentation, user agreed or Table 3 values.

6.3.2 Longitudinal conversion loss (LCL)

This parameter is also called longitudinal balance. It is a measure of how much of a common-mode signal is converted into a differential signal. This is a key measurement to assess the matching of in-line SPD series elements.

6.3.2.1 Values

The LCL value decreases with increasing frequency (see Table 3).

The test method is given in clause 7.3.2.

6.3.2.2 Criteria

The measured LCL must be within the product documentation, user agreed or Table 3 values.

6.3.3 Insertion loss

The insertion loss value represents how much signal transmission is lost by the SPD being in circuit.

6.3.3.1 Values

The insertion loss values in Table 3 cover SPDs with and without series overcurrent protectors.

The test method is given in clause 7.3.3.

6.3.3.2 Criteria

The measured insertion loss must not be greater than the product documentation, user agreed or Table 3 values.

6.3.4 Return loss

The return loss value represents how much the effective port input impedance deviates from the characteristic or nominal impedance of the network.

6.3.4.1 Values

The return loss value should be consistent over the frequency range of interest (see Table 3).

The test method is given in clause 7.3.4.

6.3.4.2 Criteria

The measured return loss must not be less than the product documentation, user agreed or Table 3 values.

Table 3 – SPD signal characteristics

Typical application	POTS	ADSL	VDSL	VDSL2	
Characteristic					Conditions
Capacitance ^{a)} pF	<200	<40	<35	<10	1 MHz, 1 V _{rms} 0 V DC
Longitudinal conversion loss ^{a)} (LCL) dB	> 60	>60	>60	>60	<1 kHz @ 600 Ω
	>55	>55	>55	>55	1 kHz-10 kHz @ 600 Ω
	>50	>50	>50	>50	10 kHz-100 kHz @ 600 Ω
	–	>18	>18	>18	7 MHz @ 100 Ω
Insertion loss ^{a)} dB	<0.5	<0.5	<0.5	<0.5	300 Hz-100 kHz @ 600 Ω
	–	<1.5	<1.5	<1.5	7 MHz @ 100 Ω
Return loss ^{a)} dB	>12	>12	>12	>12	300 Hz-100 kHz @ 600 Ω
	–	>12	>12	>12	7 MHz @ 100 Ω
^{a)} Alternatively, product documentation values or user agreed values may be used.					

6.4 Ratings

Ratings are usually verified. The rated parameter value is applied to the SPD; then, after the test, the SPD is checked for degradation.

6.4.1 Rated peak impulse current

The rated peak impulse current is the maximum level of a defined impulse that may be applied without causing degradation or failure.

6.4.1.1 Values

There are many waveshapes that are used for impulse ratings. Two common long duration waveshapes are 10/700 and 10/1000. The applied impulse levels are given in Table 4.

The test method is given in clause 7.4.1.

6.4.1.2 Criteria

After the test the SPD shall still meet its insulation resistance and maximum limiting voltage values.

Table 4 – Rated peak impulse current

Impulse	Mode	Figure	Basic	Enhanced
10/700	Transverse	3	100 A (4 kV) 5/320	150 A (6 kV) 5/320
10/1000	Transverse	3	100 A (1 kV) 10/1000	200 A (2 kV) 10/1000
10/700	Longitudinal	4	2 × 72 A (4 kV) 4/250	2 × 109 A (6 kV) 4/250
10/1000	Longitudinal	4	2 × 100 A (1 kV) 10/1000	2 × 200 A (2 kV) 10/1000

6.4.2 Impulse durability

Thyristor-based SPDs tend to show any wear-out mechanism after some 10 s of impulses. Durability tests need only be run for a hundred or more impulses in each polarity to prove durability.

6.4.2.1 Values

Table 5 shows the test levels and number of test cycles for transverse and longitudinal modes for 10/700 or 10/1000 impulses. The country an SPD is to be used in will determine the impulse durability test waveshape.

The test method is given in clause 7.4.2.

6.4.2.2 Criteria

After the durability test, the SPD should still meet its insulation and voltage limiting requirements.

6.4.3 AC durability

Each AC durability test subjects the SPD to many AC cycles. During each test there will be a thermal accumulation and after the test a check is made for any SPD degradation.

6.4.3.1 Values

The AC 50/60 Hz row of Table 5 shows the three sets of rms current, test time and AC applications associated with the basic and enhanced current columns. The SPD is to be tested for all three sets of test conditions of the chosen basic or enhanced column.

The test method is given in clause 7.4.3.

6.4.3.2 Criteria

After the durability test, the SPD should still meet its insulation resistance and voltage limiting requirements.

Table 5 – Durability test levels

Waveshape	Mode	Figure	Basic current	Enhanced current	Applications
10/700	Transverse	3	100 A (4 kV) 5/320	150 A (6 kV) 5/320	150 in each polarity
10/1000	Transverse	3	100 A (1 kV) 10/1000	200 A (2 kV) 10/1000	100 in each polarity
10/700	Longitudinal	4	2 × 72 A (4 kV) 4/250	2 × 109 A (6 kV) 4/250	150 in each polarity
10/1000	Longitudinal	4	2 × 100 A (1 kV) 10/1000	2 × 200 A (2 kV) 10/1000	100 in each polarity
AC 50/60 Hz ^{a)}	Longitudinal	17	10 A rms for 1 s	15 A rms for 1 s	5
			1 A rms for 1 s	1.5 A rms for 1 s	60
			0.5 A rms for 30 s	1 A rms for 30 s	1
^{a)} AC voltage must be sufficiently high to cause SPD conduction for at least 120° of each half cycle.					

6.5 Overload parameters

The SPD, when tested to clause 7.5, can only fail in a short circuit or low resistance mode. The SPD should not cause a safety hazard such as catching on fire, ejection of materials, including ejection from any socket.

Table 6 – Overload impulse and power fault test levels

Waveshape	Mode	Figure	Level
8/20	Longitudinal	16	2 × 5 kA; one impulse test in each polarity ^{a)}
AC 50 Hz or 60 Hz	Longitudinal	17	2 × 25 A short-circuit current for 15 min at the local AC mains voltage ^{a)}
^{a)} Alternatively, product documentation values or user agreed values may be used.			

6.5.1 High impulse current

The SPD port input terminals are simultaneously subjected to specified amplitude 8/20 current impulses in Table 6. Two impulse tests are applied, one in each polarity.

6.5.1.1 Values

Table 6 lists the applied test conditions.

The test method is given in clause 7.5.1.

6.5.1.2 Criteria

Any SPD in failure shall be a short circuit or low resistance. The SPD should not cause a safety hazard such as catching on fire, ejection of materials, including ejection from any socket.

6.5.2 Power fault

The SPD port input terminals are simultaneously subjected to specified amplitude AC power fault condition.

6.5.2.1 Values

Table 6 lists the applied test conditions.

The test method is given in clause 7.5.2.

6.5.2.2 Criteria

Any SPD in failure shall be a short circuit or low resistance. The SPD should not cause a safety hazard such as catching on fire, ejection of materials, including ejection from any socket. There shall be no externally visible damage.

7 Test methods

For these tests, the SPD should be mounted as detailed in the product documentation or user agreement.

Unless otherwise specified, all tests shall be carried out under standard atmospheric conditions for testing as given in clause 5.3 of [b-IEC 60068-1]:

- temperature 15°C to 35°C;
- relative humidity 25% to 75%;
- air pressure 86 kPa to 106 kPa.

With the exception of capacitance, all other thyristor parameters are temperature sensitive. The characteristic values follow physical laws and the change with temperature can be predicted. Clause 6 gives indications on how the characteristics vary. Ratings involve high current operation and the parameter variation is not very predictable. For rigorous designs, the SPD performance should be checked at the maximum and minimum operating temperatures of the intended application.

The impulse generators used for testing are detailed in Annex A.

7.1 Characteristics

7.1.1 Impulse voltage limiting

This test measures the SPD limiting voltage for the following conditions:

- a) Rated peak impulse current
 - 1) transverse mode, both input terminals, both impulse polarities (Figure 3)
 - 2) longitudinal mode, both impulse polarities (Figure 4);
- b) Fast impulse
 - 1) transverse mode, both input terminals, both impulse polarities (Figure 5)
 - 2) longitudinal mode, both impulse polarities (Figure 6).

7.1.1.1 Transverse mode rated peak impulse current voltage limiting

Figure 3 shows the test circuit used. Ganged switches S1 and S2 short one input terminal and feed the impulse to the other input terminal. An impulse is applied in switch position 1 and then repeated with the switch in position 2. The polarity of the generator impulse is then changed. The impulses are then repeated with the switches in positions 1 and 2. For each impulse the peak residual impulse voltage occurring at the output terminal is recorded, in switch position 1 voltage V_1 and switch position 2 voltage V_2 .

The impulse generator short-circuit amplitude is set to SPD rated current level. To avoid thermal accumulation, allow at least a one or two second waiting time between impulses.

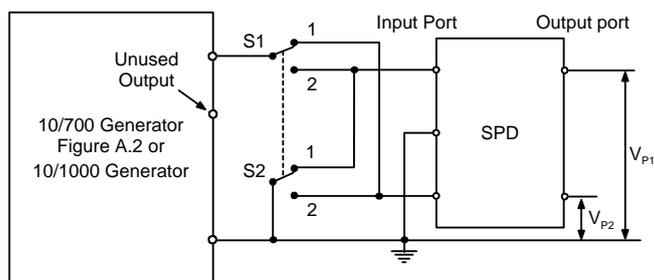


Figure 3 – Transverse impulse rating verification and limiting voltage measurement

7.1.1.2 Longitudinal mode rated peak impulse current voltage limiting

Figure 4 shows the test circuit used. The two generator outputs directly connect to the SPD input terminals. An impulse is applied in one polarity and then repeated in the opposite polarity. For each impulse the peak residual impulse voltages occurring at the output terminals, V_1 and V_2 , are recorded.

The impulse generator short-circuit amplitude is set to SPD rated current level. To avoid thermal accumulation allow at least a one or two second waiting time between impulses.

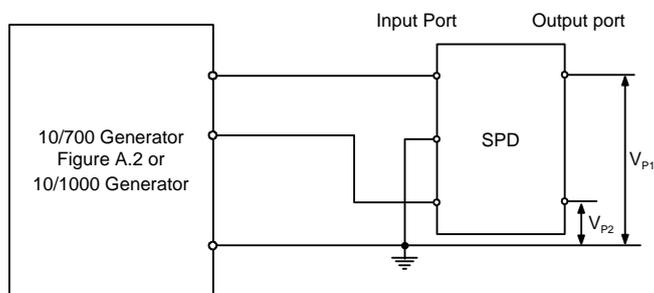


Figure 4 – Longitudinal impulse rating verification and limiting voltage measurement

7.1.1.3 Transverse mode fast impulse voltage limiting

Figure 5 shows the test circuit used. Ganged switches S1 and S2 short one input terminal and feed the impulse to the other input terminal. An impulse is applied in switch position 1 and then repeated with the switch in position 2. The polarity of the generator impulse is then changed. The impulses are then repeated with the switches in positions 1 and 2. For each impulse the peak residual impulse voltage occurring at the output terminal is recorded, in switch position 1 voltage V_1 and switch position 2 voltage V_2 .

To maintain the same waveform as the longitudinal mode test current sharing resistor R_2 is connected to earth. The generator charging voltage is adjusted to give the same amplitude impulse as the longitudinal mode rated peak impulse current. To avoid thermal accumulation allow at least a one or two second waiting time between impulses.

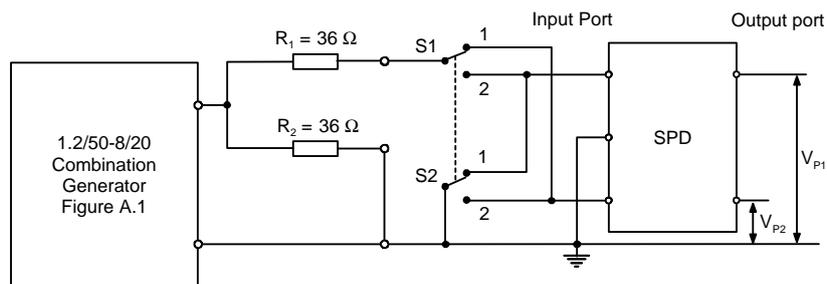


Figure 5 – Transverse fast limiting voltage measurement using a 1.2/50-8/20 generator

7.1.1.4 Longitudinal mode fast impulse voltage limiting

Figure 6 shows the test circuit used. The two current shared generator outputs (R_1 and R_2) directly connect to the SPD input terminals. An impulse is applied in one polarity and then repeated in the opposite polarity. For each impulse the peak residual impulse voltages occurring at the output terminals, V_1 and V_2 , are recorded.

The generator charging voltage is adjusted to give the same amplitude impulse as the longitudinal mode rated peak impulse current. To avoid thermal accumulation allow at least a one or two second waiting time between impulses.

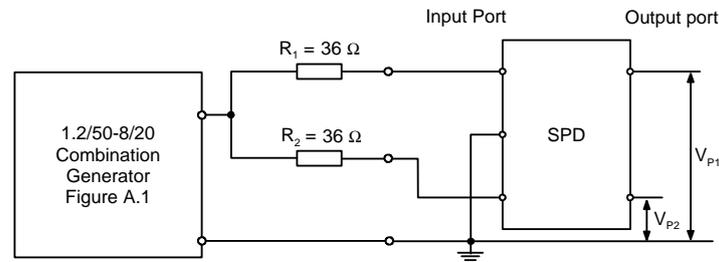


Figure 6 – Longitudinal fast limiting voltage measurement using a 1.2/50-8/20 generator

7.1.2 Leakage current

Figure 7 shows the test circuit used. The specified SPD insulation test voltage, V_{IR} , is applied with the switch S in position 1 and position 2. The leakage current that flows, I_{IR} , in each switch position is recorded. The insulation resistance test voltage polarity is then reversed and leakage current, I_{IR} , in each switch position is recorded.

Terminals not involved in the measurement are left floating.

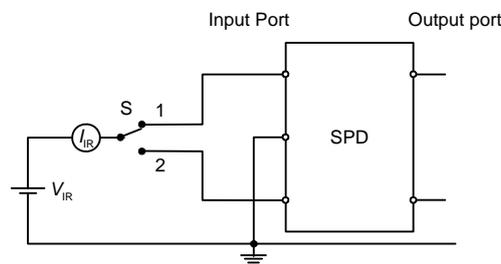


Figure 7 – Measurement of leakage current, I_{IR} , to determine insulation resistance

7.1.3 Holding current

Figure 8 shows the test circuit used. The positive polarity impulse from the generator, via diode D_1 , switches the SPD into a low-voltage condition. The low-voltage condition, usually just few volts, draws additional current, via diode D_2 , from the bias circuit of R and V_{BAT} . In the low-voltage condition the SPD conducts both the impulse current and the bias circuit current. After the impulse current ends, the only current available to hold the SPD in a low-voltage condition is the bias circuit current. The bias current is set to the SPD specified minimum holding current I_h . The SPD passes the test if it switches off after the impulse ends. The non-conducting condition can be determined by monitoring the output terminal voltage. If it is nearly the V_{BAT} voltage value, then the SPD has switched off.

The test is then repeated with the SPD terminal connections transferred to the untested terminals. The bias voltage and impulse polarities are then changed together with reversing the diode connections (poling). The test sequence is then repeated to check the holding currents in the opposite polarity.

The maximum short-circuit impulse current should be 25 A, from a 10/1000 or 10/700 generator. As shown, impulse current should be applied to the SPD in the same polarity as the bias voltage.

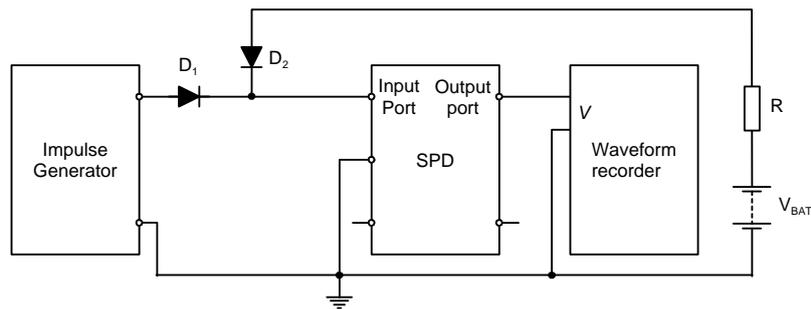


Figure 8 – Holding current test circuit

7.2 Series element characteristics

The test approaches used in this clause are based on [ITU-T K.82], but with modifications to avoid premature activation of the SPD overvoltage protection thyristor.

7.2.1 Hold current, I_H

The in-line SPD shall be connected and enclosed in a chamber as in Figure 9. The chamber temperature is adjusted to the value given for this test in the product documentation and the air allowed to become stationary.

The SPD input terminals are connected to constant current supplies set to the appropriate I_H value either from Table 2, the product documentation or the user agreed value. The maximum open-circuit voltage of a supply shall not exceed the insulation resistance test voltage V_R . The input port terminal voltages, V_1 and V_2 , are measured for the specified test time. If no time is specified, the default test time is 30 minutes. For ECLs, the default time is 200 s. Bidirectional ECLs are to be tested twice, once in each polarity as they are not necessarily symmetrical in I_H value.

The SPD series element has tripped if the measured voltage exceeds 90% of the supply open-circuit voltage.

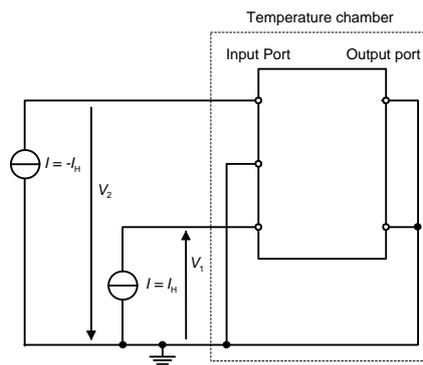


Figure 9 – Hold current verification circuit

7.2.2 Trip current, I_t

The in-line SPD shall be connected and enclosed in a chamber as in Figure 10. The chamber temperature is adjusted to the value given for this test in the product documentation and the air allowed to become stationary.

The SPD input terminals are connected to constant current supplies set to the appropriate I_t value either from Table 2, the product documentation or the user agreed value. The maximum open-circuit voltage of a supply shall not exceed the insulation resistance test voltage, V_R . The input port terminal voltages, V_1 and V_2 , are measured for the specified test time. If no time is specified, the default test time shall be 30 minutes; if tripping occurs the test may be terminated. For ECLs, the default time is 2 s. Bidirectional ECLs are to be tested twice, once in each polarity as they are not necessarily symmetrical in I_t value.

The SPD series element has tripped if the measured voltage exceeds 90% of the supply open-circuit voltage.

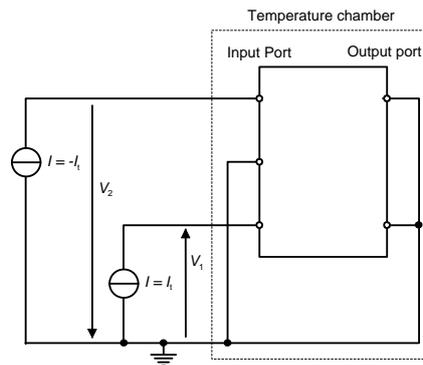


Figure 10 – Trip current verification circuit

7.2.3 Time-to-trip, $t_{\text{trip}} @ I_{\text{fault}}$

This test is for in-line SPDs using PTC thermistor self-restoring overcurrent protection elements. The in-line SPD shall be connected and enclosed in a chamber as in Figure 11. The chamber temperature is adjusted to the value given for this test in the product documentation and the air allowed to become stationary.

The SPD input terminals are connected to constant current supplies set to the appropriate I_{fault} value either from Table 2, the product documentation or the user agreed value. The maximum open-circuit voltage of a supply shall not exceed the insulation resistance test voltage, V_R . The input port terminal voltages, V_1 and V_2 , are measured for the specified test time. The current sources should reach 90% of the fault current value within 1 ms of the test start.

The SPD series element has tripped if the measured voltage exceeds 90% of the supply open-circuit voltage. The trip event time shall be recorded. This test shall be repeated for various values of I_{fault} between $2I_t$ and the level of I_{fault} that causes the series element voltage to be 90% of the supply open-circuit voltage.

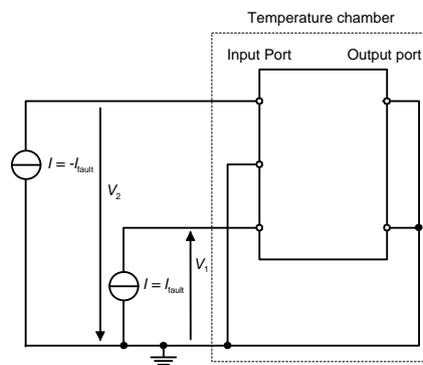


Figure 11 – Time to trip measurement circuit

7.2.4 Impulse let-through current

This test is for in-line SPDs using self restoring PTC thermistor overcurrent protection elements. The in-line SPD shall be connected into the Figure 12 circuit. Both the SPD output terminals are shorted and the currents, I_1 and I_2 , monitored. Resistors R_3 and R_4 convert the single output of the 1.2/50-8/20 surge generator into two to connect to the SPD individual input terminals. The resistor values used create an effective impulse source impedance of $40\ \Omega$ at each input terminal. The resistor values may need to be increased for SPDs with V_{IR} values below 200 V for finer adjustment. The generator charging voltage should be set to a low level, approximately 100 V, and the SPD surged. The monitored currents should show a double exponential waveform. The generator voltage should then be progressively increased and the impulse currents monitored. When the current waveform becomes truncated due to the overvoltage protection operating, the peak let-through current shall be recorded.

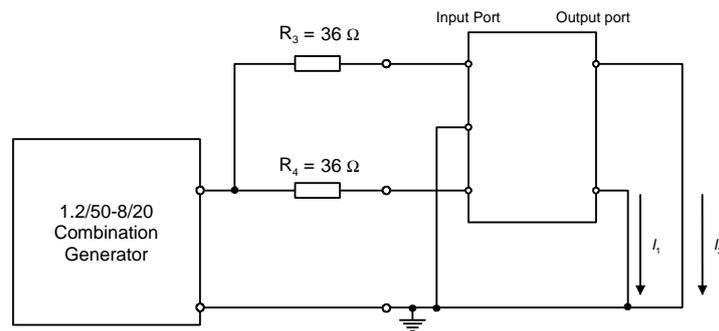


Figure 12 – Impulse let-through current measurement circuit

7.3 Signal characteristics

The measurement of signal characteristics uses a network analyser as described in [b-IEC 61643-21].

7.3.1 Capacitance

The capacitance of a port terminal and the SPD earth terminal may be measured directly on a capacitance meter or a network analyser.

7.3.2 Longitudinal conversion loss (LCL)

The network analyser signal is applied in common mode to the SPD by the common mode injector. The resultant differential signal is extracted by the longitudinal balance bridge as the input back to the network analyser. Matching to the coaxial cable impedance is done by the appropriate selection of the impedance Z_0 .

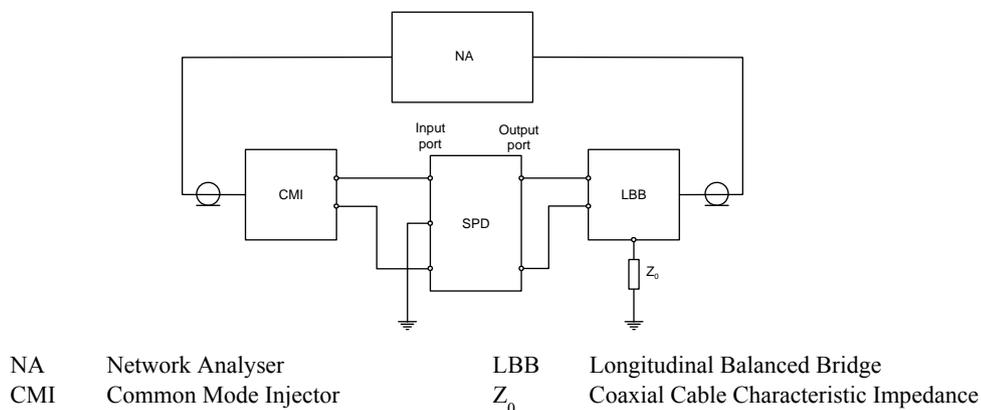


Figure 13 – Longitudinal conversion loss measurement circuit

7.3.3 Insertion loss

The signal from the network analyser is converted to a balanced signal to the SPD by a balun transformer. The signal from the SPD output is converted back to an unbalanced signal to the signal analyser by a second balun transformer. The signal level returned to the analyser, with and without the SPD in circuit, allows the insertion loss to be measured.

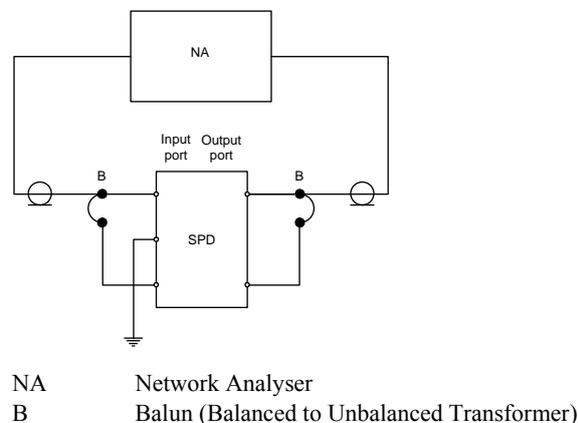


Figure 14 – Insertion loss measurement circuit

7.3.4 Return loss

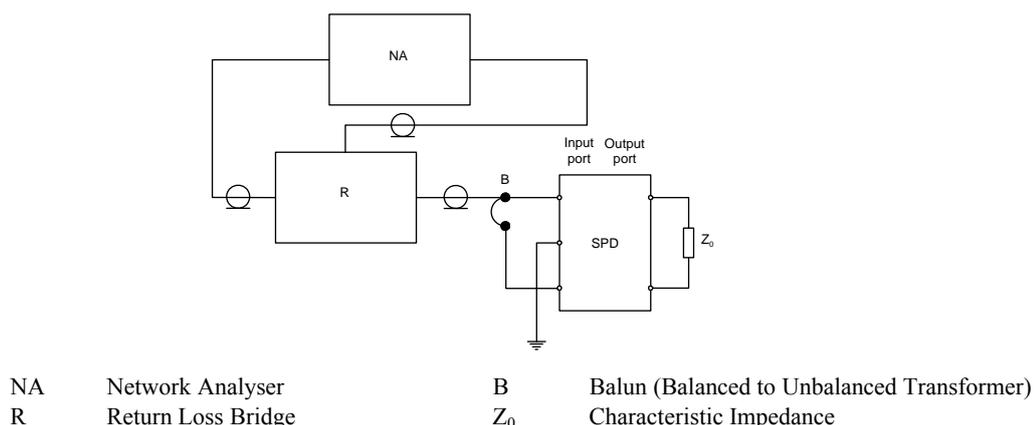


Figure 15 – Return loss measurement circuit

7.4 Rating tests

7.4.1 Rated peak impulse current

These tests are performed in the same manner as the rated peak impulse current voltage limiting tests (clauses 7.1.1.1 and 7.1.1.2, Figures 3 and 4) with the exception that the limiting voltage is not measured. The number of test impulses shall be 5 in each polarity and connection mode. After all the impulse tests, the SPD leakage current (clause 7.1.2) is measured and the insulation resistance calculated as a degradation check.

7.4.2 Impulse durability

Thyristor-based SPDs tend to show any wear-out mechanism after some 10 s of impulses. Durability tests need only be run for a hundred or more impulses in each polarity to prove durability.

The test circuits used are Figures 3 and 4 and the testing is done in the same manner as clause 7.4.1 with the exception that the number of impulses is increased to the number specified in Table 5. In addition to the post-test leakage current measurement, the limiting voltage is also measured.

7.4.3 AC durability

Figure 17 shows the test circuit for AC durability. The test values to be used are shown in Table 5. The value of AC voltage used must be sufficiently high to cause SPD conduction for at least 120° of each half cycle. Resistors R1 and R2 set the maximum current level. During each test there will be a thermal accumulation and there must be sufficient time between tests to allow for thermal stabilization back to ambient temperature. After the testing, leakage current and limiting voltage are measured as a degradation check.

7.5 Overload parameters

7.5.1 High impulse current

Figure 16 shows the test circuit. The SPD port input terminals are simultaneously subjected to specified amplitude 8/20 current impulses in Table 6. Two impulse tests are applied, one in each polarity.

During the test the SPD is monitored for any safety hazards such as catching on fire, ejecting materials, including ejection from any socket. There shall be no externally visible damage.

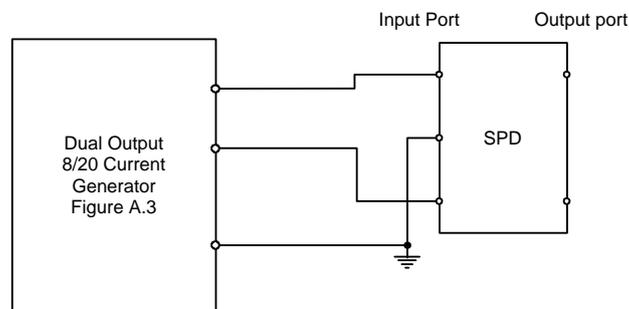


Figure 16 – Overstress surge test circuit

7.5.2 Power fault

Figure 17 shows the test circuit. The SPD port input terminals are simultaneously subjected to specified amplitude AC levels and times shown in Table 6. The value of AC voltage used must be sufficiently high to cause SPD conduction for at least 120° of each half cycle. Resistors R1 and R2 set the maximum current levels.

During the test the SPD is monitored for any safety hazards such as catching on fire, ejecting materials, including ejection from any socket. There shall be no externally visible damage.

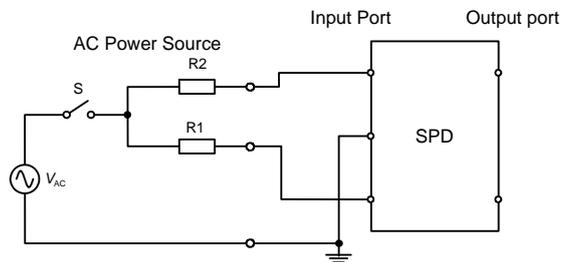


Figure 17 – Power fault test circuit

8 Identification

8.1 Marking

Legible and permanent marking shall be applied to the SPD, as necessary, to ensure that the user can determine the following information by inspection:

- a) manufacturer;
- b) year of manufacture;
- c) device number or code.

If requested and agreed, the customer's identification should be marked on each device.

8.2 Documentation

Documents shall be provided to the user so that from the information in clause 8.1, the user can determine the following additional information:

- a) appropriate device parameters as set out in this Recommendation;
- b) component mounting requirements and processes.

9 Ordering information

The following information should be supplied by the user:

- a) drawing giving all dimensions, finishes and termination details;
- b) type or model;
- c) quantity;
- d) quality assurance requirements.

Annex A

Impulse generators

(This annex forms an integral part of this Recommendation.)

A.1 Introduction

This Recommendation refers to four types of impulse generator. This annex provides more details on these generators.

A.2 Waveform tolerances

Table A.1 lists the generator open-circuit voltage and short-circuit current tolerances

Table A.1 – Waveforms of impulse generators

Designation	Condition	Edge	Time and tolerance	Amplitude
1.2/50-8/20 ^{a)} [b-IEC 61000-4-5]	Open-circuit voltage	Front	1.2 $\mu\text{s} \pm 30\%$	$\pm 10\%$
		Decay	50 $\mu\text{s} \pm 20\%$	
	Short-circuit current	Front	8 $\mu\text{s} \pm 20\%$	$\pm 10\%$ 0 to -30% undershoot
		Decay	20 $\mu\text{s} \pm 20\%$	
10/700 ^{b)} [b-IEC 61000-4-5] [b-ITU-T K.44]	Open-circuit voltage	Front	10 $\mu\text{s} \pm 30\%$	$\pm 10\%$
		Decay	700 $\mu\text{s} \pm 20\%$	
	Short-circuit current	Front	5 $\mu\text{s} \pm 20\%$	$\pm 10\%$
		Decay	320 $\mu\text{s} \pm 20\%$	
<10/>1000 ^{c)} [b-GR-1089-CORE]	Open-circuit voltage	Front	10 $\mu\text{s} -40\%$ to 0	0 to $+15\%$
		Decay	1000 μs 0 to $+50\%$	
	Short-Circuit Current	Front	10 $\mu\text{s} -40\%$ to 0	0 to $+15\%$
		Decay	1000 μs 0 to $+50\%$	
8/20 [b-IEC 62475]	Open-circuit voltage ^{d)}			
	Short-circuit current	Front	8 $\mu\text{s} \pm 10\%$	$\pm 10\%$ 0 to -20% undershoot
		Decay	20 $\mu\text{s} \pm 10\%$	
^{a)} The 1.2/50-8/20 generator effective impedance is $2 \Omega \pm 10\%$. ^{b)} The 10/700 generator short-circuit current waveshape is 5/320 for single output and 4/250 for dual output. The dual output current tolerance is 4 $\mu\text{s} \pm 20\%$ front, 250 $\mu\text{s} \pm 20\%$ duration and $\pm 10\%$ amplitude. ^{c)} The <10/>1000 generator waveform tolerances apply for both single and dual output. ^{d)} Voltage waveshape not defined. Usually the peak charging voltage for the specified 8/20 current value is given.				

A.3 1.2/50 – 8/20 impulse generator

This generator is used to determine the fast rate of rise limiting voltage and verify the SPD has a di/dt capability of $90 \text{ A}/\mu\text{s}$. To perform a simultaneous test, two external 36Ω current sharing resistors are used (see Figure A.1).

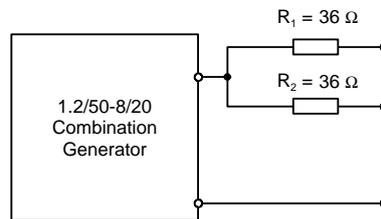


Figure A.1 – Dual output configuration of 1.2/50-8/20 combination generator

A.4 10/700 impulse generator

This generator is defined by a circuit diagram in [b-ITU-T K.44] (see Figure A.2).

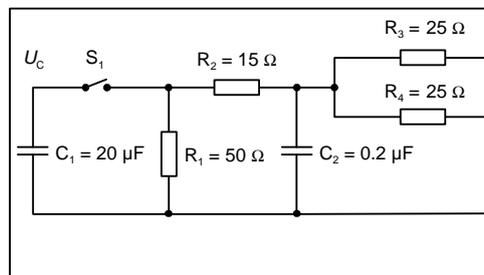


Figure A.2 – Dual output 10/700 generator

A.5 10/1000 impulse generator

The 10/1000 waveforms are defined in [b-GR-1089-CORE] and the generator is specified to have two independent outputs.

A.6 8/20 current impulse generator

The 8/20 waveform is defined in [b-IEC 62475]. Figure A.3 shows a dual output 8/20 generator that produces $2 \times 3 \text{ kA/kV}$ of charging voltage U_C and a 20% underswing. Values for 10% underswing and 2.8 kA/kV would be $L_1 = 1.5 \mu\text{H}$, $C_1 = 96 \mu\text{F}$ and $R_1 = 0.21 \Omega$.

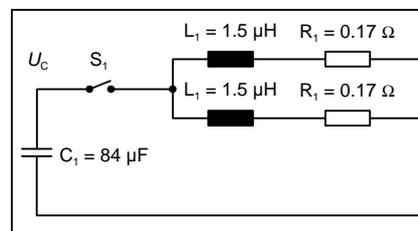


Figure A.3 – Dual output 8/20 generator

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