International Telecommunication Union

ITU-T G.707/Y.1322

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

Amendment 2
(11/2009)

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Recommendation ITU-T G.707/Y.1322

Network node interface for the synchronous digital hierarchy (SDH)

Amendment 2

Summary

Amendment 2 to Recommendation ITU-T G.707/Y.1322 contains additional material to be incorporated in the Recommendation and adds the necessary functionality for adaptation of STM-256 over multichannel parallel interfaces.

Source

Amendment 2 to Recommendation ITU-T G.707/Y.1322 (2007) was approved on 13 November 2009 by ITU-T Study Group 15 (2009-2012) under Recommendation ITU-T A.8 procedures.

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

Recommendation ITU-T G.707/Y.1322

Network node interface for the synchronous digital hierarchy (SDH)

Amendment 2

1 Modify clause 4

Add the following abbreviation to clause 4:

STL Synchronous Transport Lane

2 Modify Table 6-2

Enhance Table 6-2 with the bit-rate of an STL-256.4:

Table 6-2 – SDH hierarchical bit rates

Synchronous digital hierarchy level	Hierarchical bit rate (kbit/s)
0	51 840
1	155 520
4	622 080
16	2 488 320
64	9 953 280
256	39 813 120
STL-256.4	9 953 280
NOTE – The specification of levels higher than 256 requires further study.	

3 Add new clause 6.7

Add the following clause:

6.7 Parallel interfaces

STM-256 may be inversely multiplexed over four STL-256.4s. See Annex I for the inverse multiplexing of STM-256 over STL-256.4s. The four STL-256.4s are optically multiplexed onto a single multilane section (see Rec. ITU-T G.783).

NOTE – Interconnection of equipment that supports the newer synchronous transport lane (STL) structures with older equipment only supporting the non-STL interface defined in older versions of this Recommendation cannot be achieved automatically. For interconnection of equipment supporting the newer STL structures with older equipment only supporting the non-STL interface defined in older versions of this Recommendation, it will be necessary for the former to support the non-STL interface.

4 Insert new Annex I

Add the following annex:

Annex I

Adaptation of STM-256 over multichannel parallel interfaces

(This annex forms an integral part of this Recommendation)

NOTE – This mechanism is designed to allow the use of the optical modules being developed for IEEE 40GBASE-R signals for short-reach client-side STM-256 interfaces.

So that STM-256 signals may be carried over parallel interfaces consisting of four lanes, the STM-256 frame is inversely multiplexed over physical/logical lanes on a 16-byte boundary aligned with the frame as illustrated in Figure I.1.

1						69120
1	1:16	17:32	33:48	49:64		69105:69120
2	69121:69136	69137:69152	69153:69168	69169:69184		138225:138240
3	138241:138256	138257:138272	138273:138288	138289:138304		207345:207360
4	207361:207376	207377:207392	207393:207408	207409:207424		276465:276480
5	276481:276496	276497:276512	276513:276528	276529:276544	• • •	345585:345600
6	345601:345616	345617:345632	345633:345648	345649:345664		414705:414720
7	414721:414736	414737:414752	414753:414768	414769:414784		483825:483840
8	483841:483856	483857:483872	483873:483888	483889:483904		552945:552960
9	552961:552976	552977:552992	552993:553008	553009:553024		622065:622080

Figure I.1 – STM-256 frame divided on 16-byte boundary

Each 16-byte increment of the STM-256 frame is distributed, round robin, to each of the four physical lanes as illustrated in Figure I.2.

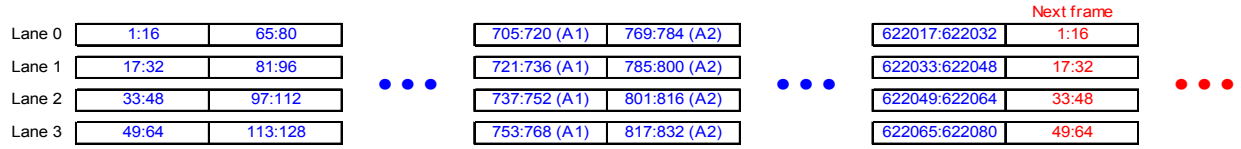

Figure I.2 – Distribution of bytes from STM-256 to parallel lanes

Since the STM-256 frame has 64 unscrambled A1 bytes followed by 64 unscrambled A2 bytes, each lane receives 16 A1 bytes followed by 16 A2 bytes. The last A2 byte position in each lane is borrowed as a logical lane marker. For maximum skew detection range, the lane marker value increments by four on successive frames (from 0 to 252 for lane 0, from 1 to 253 for lane 1, from 2 to 254 for lane 2 and from 3 to 255 for lane 3). The logical lane number can be recovered from this value by a modulo 4 operation.

Since a possible future application may re-form a single bit stream via a simple bit multiplex of the four lanes, it is necessary to delay the lanes with respect to each other to avoid the frame alignment bytes overlapping and producing a portion of the frame with very low clock content. Consequently, the lanes must be arranged to have at least 32 bytes of time offset between the A1 to A2 transition of any two of the lanes.

The parallel lanes can be reassembled at the sink by first recovering framing on each of the parallel lanes using the 16 A1 bytes followed by 15 A2 bytes. As lane positions may not be preserved by the optical modules to be used for this application, the lanes are identified using the lane marker in the byte following the fifteenth A2 byte, deskewed, and reassembled into the original STM-256 frame according to the lane marker. Since each lane marker cycles through 64 distinct values, the lanes can be deskewed and reassembled by the receiver as long as the total skew does not exceed 32 STM-256 frame periods (approximately 4 ms). In mapping from lanes back to the STM-256 frame, the byte following the fifteenth A2 byte which was borrowed for lane marking is restored to the value A2.

This mechanism handles any normally framed STM-256 sequence. The additional sequence to be handled is generic AIS, which is an unframed PN-11 sequence at the STM-256 rate. The source function for this adaptation will detect generic AIS by recognizing the PN-11 sequence.

While receiving generic AIS, the source function for distributing the STM-256 to parallel lanes will generate a framing pattern of 16 × A1 + 15 × A2 + 0xFF once per 155520 bytes at the STL bit rate as specified in Table 6-2 on each of the logical lanes. The remainder of the frame is the PN-11 pattern distributed in 16-byte increments across the lanes. When the sink function sees the lane marker fixed at 0xFF on any lane, it will generate a PN-11 sequence at the STM-256 rate in the egress direction.

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