# ITU-T

X.85/Y.1321

TELECOMMUNICATION STANDARDIZATION SECTOR OF ITU **Corrigendum 1** (06/2005)

SERIES X: DATA NETWORKS, OPEN SYSTEM COMMUNICATIONS AND SECURITY

Public data networks – Transmission, signalling and switching

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

# IP over SDH using LAPS Corrigendum 1

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# ITU-T Recommendation X.85/Y.1321

# **IP over SDH using LAPS**

### **Corrigendum 1**

#### **Summary**

This corrigendum to ITU-T Rec. X.85/Y.1321 specifies a revision of the computation of 32/16-bit FCS.

#### Source

Corrigendum 1 to ITU-T Recommendation X.85/Y.1321 (2001) was approved on 29 June 2005 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure.

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#### **ITU-T Recommendation X.85/Y.1321**

#### **IP over SDH using LAPS**

### **Corrigendum 1**

#### 1) Clause A.2.7: Frame Check Sequence (FCS) field

Modify clause A.2.7 as follow:

The FCS field shall be a 32-bit sequence. It shall be the ones complement of the sum (modulo 2) of:

- the remainder of  $x^m$  ( $x^{31} + x^{30} + ... + x + 1$ ) divided (modulo 2) by the generating polynomial, where *m* is the number of bits of the information over which the CRC is calculated; and
- the remainder of the division (modulo 2) by the generating polynomial of the product of  $x^{32}$ by the information over which the CRC is calculated. The 32-bit FCS generating polynomial is:

 $G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ 

- The result of the CRC calculation is placed with the least significant bit right justified in the FCS field. As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all "1"s and is then modified by division by the generating polynomial (as described above) on the address, control, SAPI and information fields over which the CRC is to be calculated; the ones complement of the resulting remainder is put into the 32-bit FCS field.
  - As a typical implementation at the receiver, the initial content of the register of the device computing the remainder of the division is preset to all "1"s. The final remainder, after multiplication by  $x^{32}$  and then division (modulo 2) by the generating polynomial of the serial incoming protected bits and FCS, shall be (in the absence of errors):

 $- C(x) = x^{31} + x^{30} + x^{26} + x^{25} + x^{24} + x^{18} + x^{15} + x^{14} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^4 + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^4 + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^4 + x^{12} + x^{14} + x^{12} + x^{14} + x$ 

<u>For compatibility with RFC 2615, The the computation of 32-bit FCS and 16-bit FCS is referred to carried out according to RFC 2615 for compatibility with RFC 2615</u>. In the scase of 16-bit FCS, the length of FCS is changed to the two octets in Figures A.1 and A.4.

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