ITU-R

Radiocommunication Sector of ITU

Recommendation ITU-R BT.1620-1
(03/2010)

Data structure for DV-based audio, data and compressed video at a data rate of 100 Mbit/s

BT Series

Broadcasting service
(television)

International Telecommunication Union

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Series	**Title**
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BS	Broadcasting service (sound)
BT	**Broadcasting service (television)**
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M	Mobile, radiodetermination, amateur and related satellite services
P	Radiowave propagation
RA	Radio astronomy
RS	Remote sensing systems
S	Fixed-satellite service
SA	Space applications and meteorology
SF	Frequency sharing and coordination between fixed-satellite and fixed service systems
SM	Spectrum management
SNG	Satellite news gathering
TF	Time signals and frequency standards emissions
V	Vocabulary and related subjects

Note: *This ITU-R Recommendation was approved in English under the procedure detailed in Resolution ITU-R 1.*

RECOMMENDATION ITU-R BT.1620-1

Data structure for DV-based audio, data and compressed video at a data rate of 100 Mbit/s

(Question ITU-R 12/6)

(2003-2010)

Scope

This Recommendation defines the data structure for the interface of DV-based digital audio, subcode data, and compressed video at 100 Mb/s. The standard defines the processes required to decode the DV-based data structure into eight channels of AES digital audio at 48 kHz, subcode data, and high-definition video at 1 920 × 1 080/60/I, 1920 × 1 080/50/I, 1 280 × 720/60/P and 1 280 × 720/50/P.

The ITU Radiocommunication Assembly,

considering

a)   that applications within professional television production and post-production have been identified where DV-based video compression can offer operational and economic advantages;

b)   that three data rates have been proposed within the same compression family to serve different applications (25 Mbit/s, 50 Mbit/s and 100 Mbit/s);

c)   that the sampling rasters for each of the three applications are different;

d)   that for the international exchange of high-definition programme material the ITU-R recommends the application of Recommendation ITU-R BT.709;

e)   that audio, auxiliary data and metadata elements form an integral part of these applications;

f)   that these elements are multiplexed into a single data stream for transport and further processing;

g)   that the compression quality and functional characteristics must be identical and reproducible in complex production chains;

h)   that for this purpose all details of parameters used for coding and multiplexing must be defined,

recommends

1   that for applications in professional television production and post-production using DV-based compression at 100 Mbit/s, the parameters given in Annexes 1 and 2 should be used;

2   that compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure e.g. interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words shall in no way be construed to imply partial or total compliance with this Recommendation.

Annex 1

1   Overview

This Recommendation defines how DIF packets and other data such as audio and time code data are formatted for recording on a DV-based recorder, specified elsewhere. As shown in Fig. 1, the processed audio, video and subcode data are output for the recording on a Type D-12 recorder. Additionally these data are multiplexed in the DIF (digital interface) format data to output for different applications through a digital interface port. Details of the process shown in Fig. 1 are described in § 3 and 4.

2   Abbreviations and acronyms as used in this Recommendation

AAUX	Audio auxiliary data
AP1	Audio application ID
AP2	Video application ID
AP3	Subcode application ID
APT	Track application ID
Arb	Arbitrary
AS	AAUX source pack
ASC	AAUX source control pack
CGMS	Copy generation management system
CM	Compressed macro block
DBN	DIF block number
DCT	Discrete cosine transform
DIF	Digital interface
DRF	Direction flag
Dseq	DIF sequence number
DSF	DIF sequence flag
EFC	Emphasis audio channel flag
EOB	End of block
LF	Locked mode flag
QNO	Quantization number
QU	Quantization
Res	Reserved for future use
SCT	Section type
SMP	Sampling frequency
SSYB	Subcode sync block
STA	Status of the compressed macro block

STYPE   Signal type

Syb   Subcode sync block number

TF   Transmitting flag

VAUX   Video auxiliary data

VLC   Variable length coding

VS   VAUX source pack

VSC   VAUX source control pack

References

Recommendation ITU-R BS.647 – A digital audio interface for broadcasting studios.

Recommendation ITU-R BR.780 – Time and control code standards, for production applications in order to facilitate the international exchange of television programmes on magnetic tapes.

Recommendation ITU-R BT.1847 – 1 280 × 720, 16:9 progressively-captured image format for production and international programme exchange in the 50 Hz environment.

Recommendation ITU-R BT.709 – Parameter values for the HDTV standards for production and international programme exchange.

Recommendation ITU-R BT.1543 – 1 280 × 720, 16 × 9 progressively-captured image format for production and international programme exchange in the 60 Hz environment.

Recommendation ITU-R BT.1616 – Data stream format for the exchange of DV-based audio, data and compressed video over interfaces complying with Recommendation ITU-R BT.1381.

3   Data processing

3.1   General

As shown in Fig. 1, the processed audio, video and subcode data are output for recording on a Type D-12 recorder.

3.1.1   Video encoding parameter

The source component signal to be processed shall comply with the video parameters as defined by Recommendations ITU-R BT.709, ITU-R BT.1543 and ITU-R BT.1847. Not all formats may be supported by all manufacturers.

3.1.2   Audio encoding parameter

The audio signal shall be sampled at 48 kHz, with 16-bit quantization defined by Recommendation ITU-R BS.647.

3.1.3   Subcode data

The time code format in the subcode area shall be the LTC codeword and comply with Recommendation ITU-R BR.780.

Each frame of time code shows a frame number that corresponds to each video frame in the
1 920 × 1 080-line interlaced system, and two video frames each in the 1 280 × 720-line progressive
system.

3.1.4   Frame structure

In the 1 920 × 1 080-line system, video data, audio data, and subcode data in one video frame shall
be processed in each frame. In the 1 280 × 720-line system, these data in two video frames shall be
processed within one frame duration of the 1 920 × 1 080-line system. Consequently, audio data and
subcode data in the 1 280 × 720-line system are processed in the same way as the 1 920 × 1 080-line
system. The audio data corresponding to one video frame in the 1 920 × 1 080-line system and two
video frames in the 1 280 × 720-line system is defined as an audio-processing unit.

FIGURE 1

Data processing block diagram
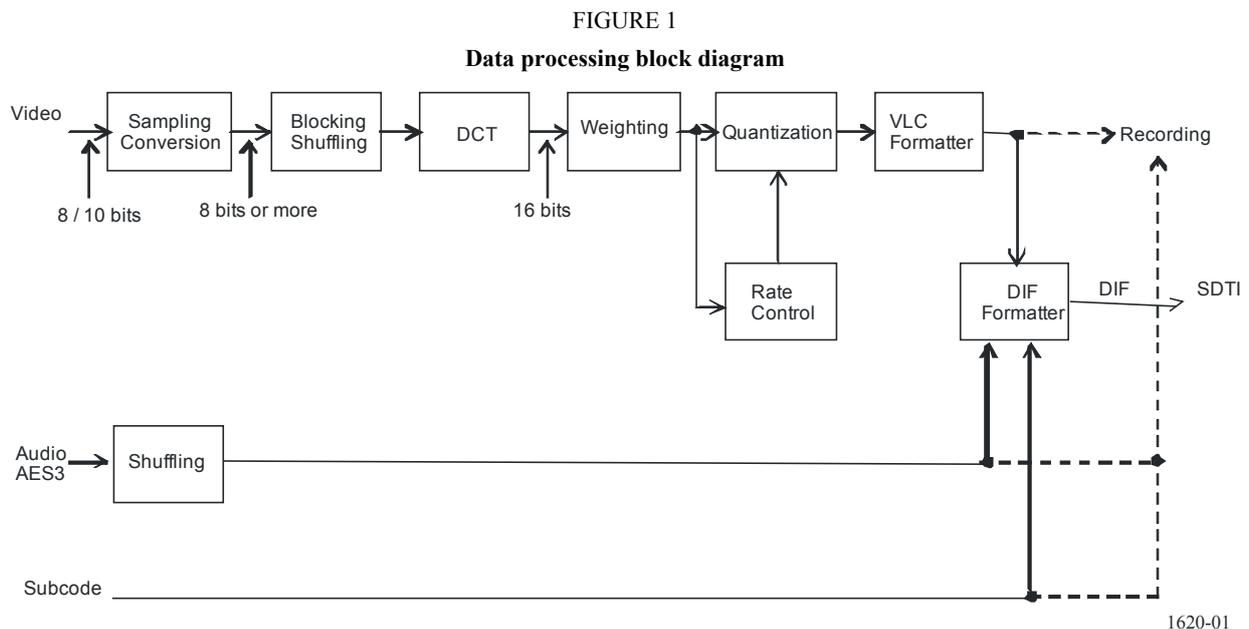
3.2   Data structure

The data structure of the compressed stream at the digital interface is shown in Fig. 2. The data of
each frame shall be divided into four DIF channels.

Each DIF channel shall be divided into 10 DIF sequences for the 60-Hz system[1] and 12 DIF
sequences for the 50-Hz system.

Each DIF sequence shall consist of a header section, subcode section, VAUX section, audio section,
and video section with the following DIF blocks respectively:

       Header section: 1 DIF block

       Subcode section: 2 DIF blocks

       VAUX section: 3 DIF blocks

       Audio section: 9 DIF blocks

       Video section: 135 DIF blocks.

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[1]   60 Hz systems also includes 60/1.001 Hz.

As shown in Fig. 2, each DIF block shall consist of a 3-byte ID and 77 bytes of data. The DIF data bytes are numbered 0 to 79. Figure 3 shows the data structure of a DIF sequence.

FIGURE 2

Data structure
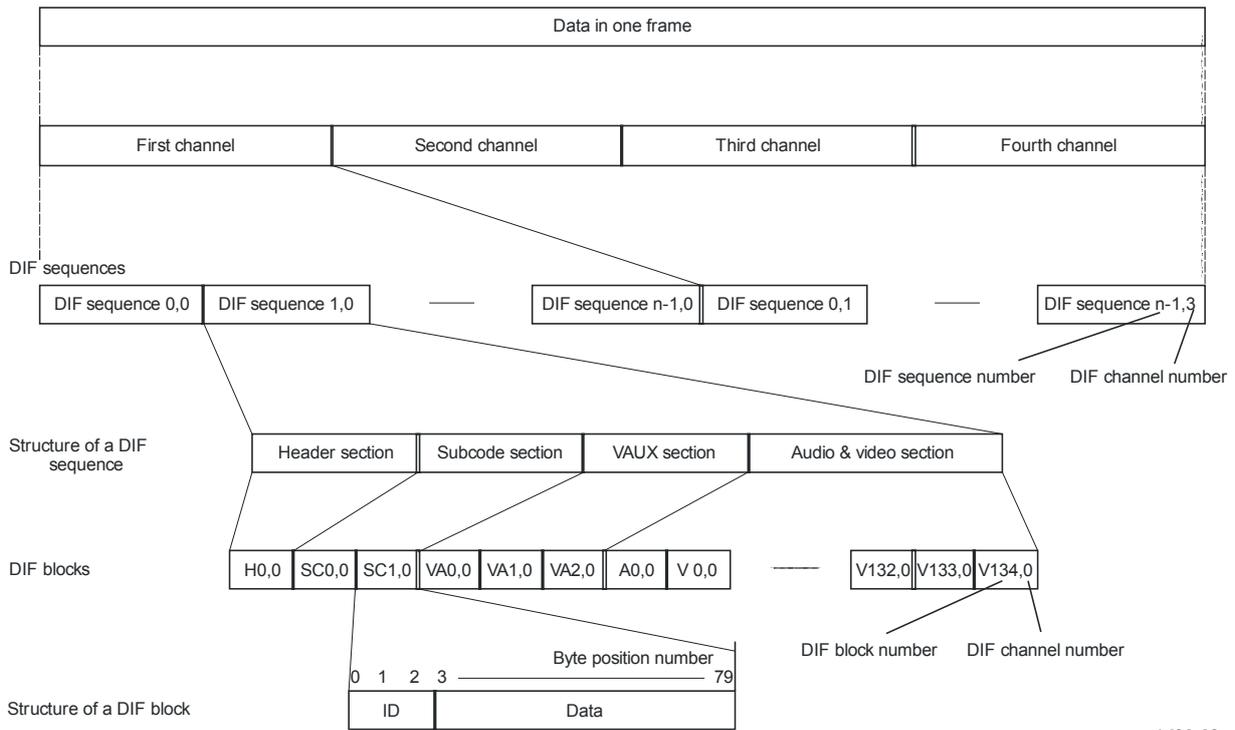
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where:

n = 10 for 60 Hz system

n = 12 for 50 Hz system.

FIGURE 3

Data structure of a DIF sequence

| DIF blocks | H0,i | SC0,i | SC1,i | VA0,i | VA1,i | VA2,i |

| A0,i | V0,i | V1,i | V2,i | V3,i | V4,i | V5,i | V6,i | V7,i | V8,i | V9,i | V10,i | V11,i | V12,i | V13,i | V14,i |

| A1,i | V15,i | V16,i | V17,i | V18,i | V19,i | V20,i | V21,i | V22,i | V23,i | V24,i | V25,i | V26,i | V27,i | V28,i | V29,i |

| A2,i | V30,i | V31,i | V32,i | V33,i | V34,i | V35,i | V36,i | V37,i | V38,i | V39,i | V40,i | V41,i | V42,i | V43,i | V44,i |

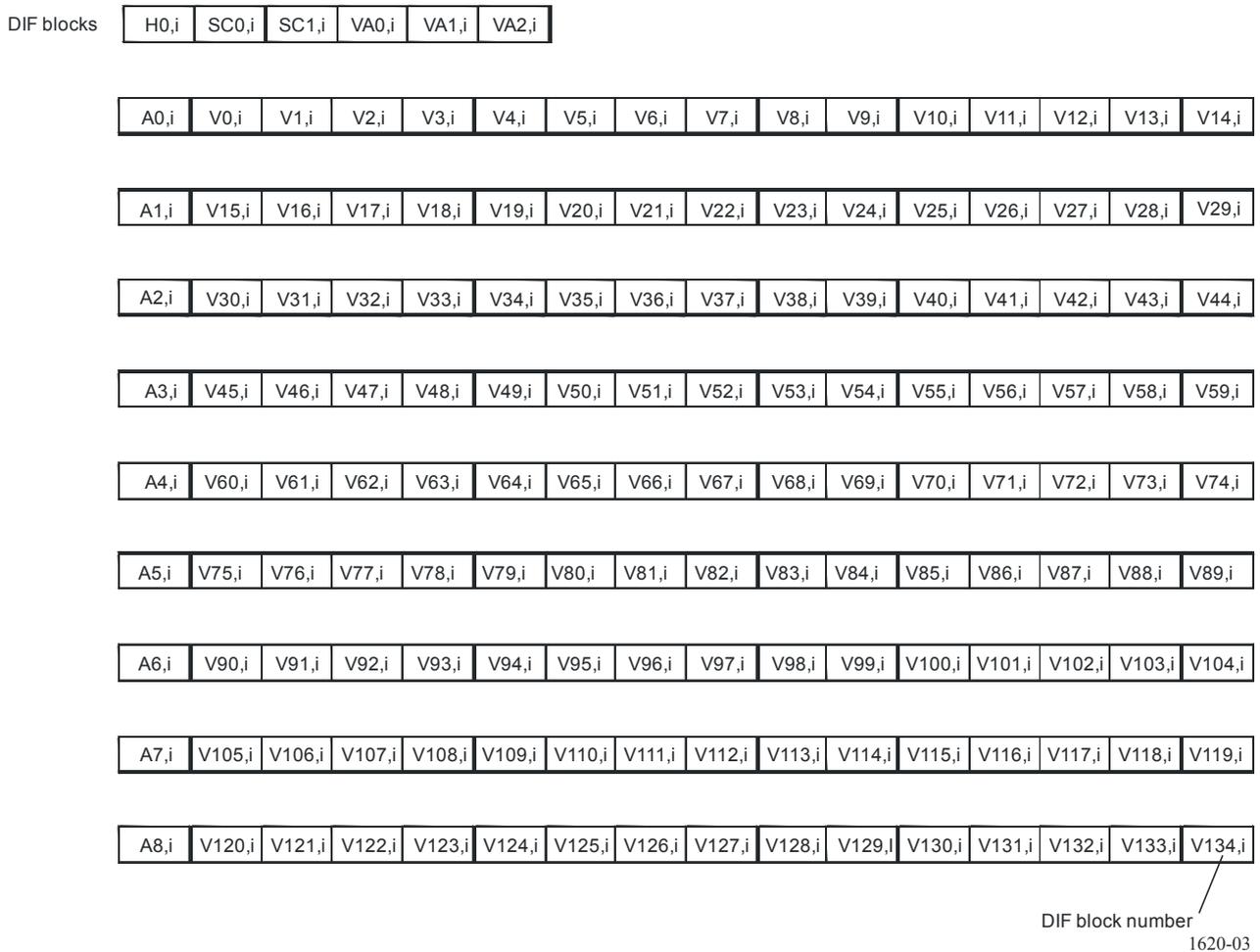| A3,i | V45,i | V46,i | V47,i | V48,i | V49,i | V50,i | V51,i | V52,i | V53,i | V54,i | V55,i | V56,i | V57,i | V58,i | V59,i |

| A4,i | V60,i | V61,i | V62,i | V63,i | V64,i | V65,i | V66,i | V67,i | V68,i | V69,i | V70,i | V71,i | V72,i | V73,i | V74,i |

| A5,i | V75,i | V76,i | V77,i | V78,i | V79,i | V80,i | V81,i | V82,i | V83,i | V84,i | V85,i | V86,i | V87,i | V88,i | V89,i |

| A6,i | V90,i | V91,i | V92,i | V93,i | V94,i | V95,i | V96,i | V97,i | V98,i | V99,i | V100,i | V101,i | V102,i | V103,i | V104,i |

| A7,i | V105,i | V106,i | V107,i | V108,i | V109,i | V110,i | V111,i | V112,i | V113,i | V114,i | V115,i | V116,i | V117,i | V118,i | V119,i |

| A8,i | V120,i | V121,i | V122,i | V123,i | V124,i | V125,i | V126,i | V127,i | V128,i | V129,I | V130,i | V131,i | V132,i | V133,i | V134,i |

DIF block number

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where:

i: DIF channel number

i = 0,1,2,3

H0,i: DIF block in header section

SC0,i to SC1,i: DIF blocks in subcode section

VA0,i to VA2,i: DIF blocks in VAUX section

A0,i to A8,i: DIF blocks in audio section

V0,i to V134,i: DIF blocks in video section.

3.3 Header section

3.3.1 ID

The ID part of each DIF block in the header section, shown in Fig. 2, shall consist of 3 bytes (ID0, ID1, ID2). Table 1 shows the ID content of a DIF block.

TABLE 1

ID data of a DIF block

	Byte position number		
	0	1	2
	ID0	ID1	ID2
MSB	SCT2	Dseq3	DBN7
	SCT1	Dseq2	DBN6
	SCT0	Dseq1	DBN5
	Res	Dseq0	DBN4
	Arb	FSC	DBN3
	Arb	FSP2	DBN2
	Arb	Res	DBN1
LSB	Arb	Res	DBN0

The ID contains the following:

SCT: Section type (see Table 2)

Dseq: DIF sequence number (see Tables 3 and 4)

FSC, FSP: Channel identification of a DIF block (see Table 5)

FSP bit is reserved

DBN: DIF block number (see Table 6)

Arb: Arbitrary bit

Res: Reserved bit for future use

Default value shall be set to 1

TABLE 2

Section type

Section type bit			Section type
SCT2	SCT1	SCT0	
0	0	0	Header
0	0	1	Subcode
0	1	0	VAUX
0	1	1	Audio
1	0	0	Video
1	0	1	Reserved
1	1	0	
1	1	1	

TABLE 3

DIF sequence number for the 60-Hz system

DIF sequence number bit				DIF sequence number
Dseq3	Dseq2	Dseq1	Dseq0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

TABLE 4

DIF sequence number for the 50-Hz system

DIF sequence number bit				DIF sequence number
Dseq3	Dseq2	Dseq1	Dseq0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

TABLE 5

DIF channel number

FSC	FSP	DIF channel number
0	1	0: first channel
1	1	1: second channel
0	0	2: third channel
1	0	3: fourth channel

TABLE 6

DIF block number

DIF block number bit								DIF block number
DBN7	DBN6	DBN5	DBN4	DBN3	DBN2	DBN1	DBN0	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
1	0	0	0	0	1	1	0	134
1	0	0	0	0	1	1	1	Not used
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	Not used

3.3.2 Data

The data part (payload) of each DIF block in the header section is shown in Table 7. Bytes 3 to 7 are active and bytes 8 to 79 are reserved.

TABLE 7

Data (payload) in the header section

Byte position number

	3	4	5	6	7	8	-------	79
MSB	DSF	Res	TF1	TF2	TF3	Res	-------	Res
	0	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	APT2	AP12	AP22	AP32	Res	-------	Res
	Res	APT1	AP11	AP21	AP31	Res	-------	Res
LSB	Res	APT0	AP10	AP20	AP30	Res	-------	Res

DSF: DIF sequence flag

0 = 10 DIF sequences included in a DIF channel (60-Hz system)

1 = 12 DIF sequences included in a DIF channel (50-Hz system)

APTn, AP1n, AP2n, and AP3n data shall be identical to the track application IDs (APTn = 001, AP1n = 001, AP2n = 001, AP3n = 001), if the source signal comes from the DV-based digital VCR. If the signal source is unknown, all bits for this data shall be set to 1.

TF: Transmitting flag

TF1: Transmitting flag of audio DIF blocks

TF2: Transmitting flag of VAUX and Video DIF blocks

TF3: Transmitting flag of subcode DIF blocks

0 = Valid data

1 = Invalid data.

Res: Reserved bit for future use

Default value shall be set to 1.

## 3.4 Subcode section

3.4.1 ID

The ID part of each DIF block in the subcode section shall be the same as described in § 3.3.1. The section type shall be 001.

3.4.2 Data

The data part (payload) of each DIF block in the subcode section is shown in Fig. 4. The subcode data shall consist of 6 SSYBs, each 48 bytes long, and a reserved area of 29 bytes in each relevant DIF block. SSYBs in a DIF sequence are numbered 0 to 11. Each SSYB shall be composed of an SSYB ID equal to 2 bytes, an FF_h, and an SSYB data payload of 5 bytes.

FIGURE 4

Data in the subcode section

1620-04
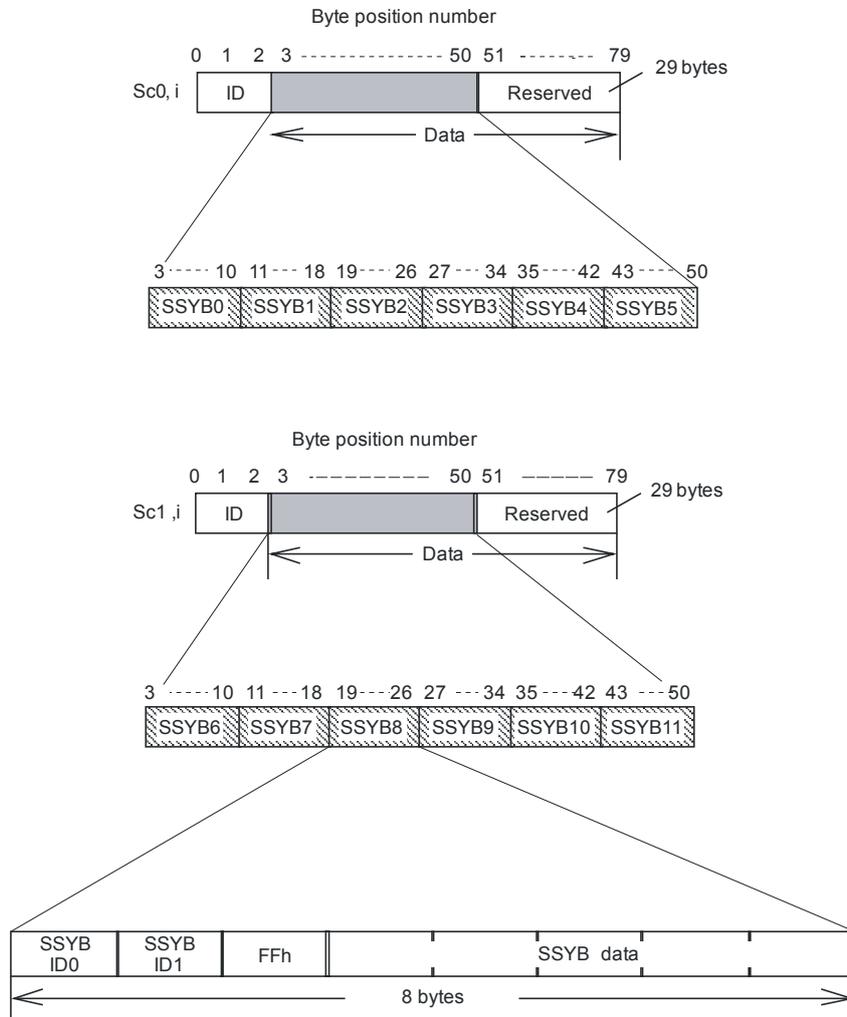
3.4.2.1   SSYB ID

Table 8 shows the parts of SSYB ID (ID0, ID1). It shall contain FR ID, application ID ($AP3_2$, $AP3_1$, $AP3_0$), (APT_2, APT_1, APT_0) and SSYB number (Syb_3, Syb_2, Syb_1, Syb_0).

TABLE 8

SSYB ID

Bit position	SSYB number 0 and 6		SSYB number 1 to 5 and 7 to 10		SSYB number 11	
	ID0	ID1	ID0	ID1	ID0	ID1
b7	FR	Arb	FR	Arb	FR	Arb
b6	AP32	Arb	Res	Arb	APT2	Arb
b5	AP31	Arb	Res	Arb	APT1	Arb
b4	AP30	Arb	Res	Arb	APT0	Arb
b3	Arb	Syb3	Arb	Syb3	Arb	Syb3
b2	Arb	Syb2	Arb	Syb2	Arb	Syb2
b1	Arb	Syb1	Arb	Syb1	Arb	Syb1
b0	Arb	Syb0	Arb	Syb0	Arb	Syb0
NOTE – Arb = arbitrary bit						

FR : The identification for the first half or second half of each DIF channel.
    1 = the first half of each DIF channel
    0 = the second half of each DIF channel

    The first half of each DIF channel
        DIF sequence number 0, 1, 2, 3, 4 for 60-Hz system
        DIF sequence number 0, 1, 2, 3, 4, 5 for 50-Hz system

    The second half of each DIF channel
        DIF sequence number 5, 6, 7, 8, 9 for 60-Hz system
        DIF sequence number 6, 7, 8, 9, 10, 11 for 50-Hz system

If information is not available, all bits shall be set to 1.

3.4.2.2   SSYB data

Each SSYB data payload shall consist of a pack of 5 bytes as shown in Fig. 5. Table 9 shows the pack header table (PC0 byte organization). Table 10 shows the pack arrangement in SSYB data for each DIF channel.
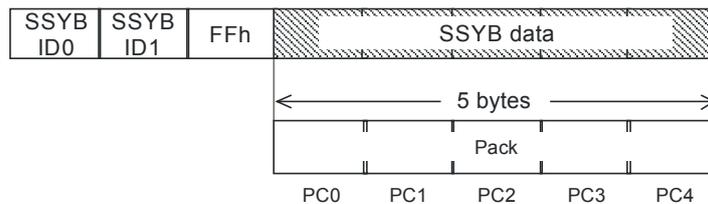
FIGURE 5

Pack in SSYB

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TABLE 9

Pack header table

UPPER / LOWER	0000	0001	0010	0011	0100	0101	0110	0111	—	1111
0000						AUDIO SOURCE	VIDEO SOURCE			
0001						AUDIO SOURCE CONTROL	VIDEO SOURCE CONTROL			
0010										
0011		TIME CODE								
0100		BINARY GROUP								
0101										
|										
1111										NO INFO

TABLE 10

Mapping of packets in SSYB data

SSYB number	The first half of each DIF channel	The second half of each DIF channel
0	Reserved	Reserved
1	Reserved	Reserved
2	Reserved	Reserved
3	TC	TC
4	BG	Reserved
5	TC	Reserved
6	Reserved	Reserved
7	Reserved	Reserved
8	Reserved	Reserved
9	TC	TC
10	BG	Reserved
11	TC	Reserved

NOTES

1 TC = Time code pack.

2 BG = Binary group pack.

3 Reserved = Default value of all bits shall be set to 1.

4 TC and BG data are the same within each frame.

   The time code data are an LCT type.

3.4.2.2.1 Time code pack (TC)

Table 11 shows the structure of the time code pack. The time code data mapped to the time code packs shall be the same within each frame.

TABLE 11

Structure of time code pack
60-Hz system

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	DF	TENS of FRAMES		UNITS of FRAMES			
PC2	PC	TENS of SECONDS			UNITS of SECONDS			
PC3	BGF0	TENS of MINUTES			UNITS of MINUTES			
PC4	BGF2	BGF1	TENS of HOURS		UNITS of HOURS			

50-Hz system

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	Arb	TENS of FRAMES		UNITS of FRAMES			
PC2	BGF0	TENS of SECONDS			UNITS of SECONDS			
PC3	BGF2	TENS of MINUTES			UNITS of MINUTES			
PC4	PC	BGF1	TENS of HOURS		UNITS of HOURS			

NOTE – Detailed information is given in ITU-R BR 780

CF: Colour frame
    0 = unsynchronized mode
    1 = synchronized mode
DF: Drop frame flag
    0 = Nondrop frame time code
    1 = Drop frame time code
PC: Biphase mark polarity correction
    0 = Even
    1 = Odd
BGF: Binary group flag
Arb: Arbitrary bit

3.4.2.2.2 Binary group pack (BG)

Table 12 shows the structure of the binary group pack. The binary group data mapped to the binary group packs shall be the same within each frame.

TABLE 12

Structure of binary group pack

	MSB							LSB
PC0	0	0	0	1	0	1	0	0
PC1	BINARY GROUP2				BINARY GROUP1			
PC2	BINARY GROUP4				BINARY GROUP3			
PC3	BINARY GROUP6				BINARY GROUP5			
PC4	BINARY GROUP8				BINARY GROUP7			

3.5   VAUX section

3.5.1   ID

The ID part of each DIF block in the VAUX section shall be the same as described in § 3.3.1. The section type shall be 010.

3.5.2   Data

The data part (payload) of each DIF block in the VAUX section is shown in Fig. 6. This figure shows the VAUX pack arrangement for each DIF sequence.

There shall be 15 packs, each 5 bytes long, and two reserved bytes in each VAUX DIF block payload. A default value for the reserved byte shall be set to FF_h.

Therefore, there are 45 packs in a DIF sequence. The VAUX packs in the DIF blocks are sequentially numbered 0 to 44. This number is called a video pack number.

FIGURE 6

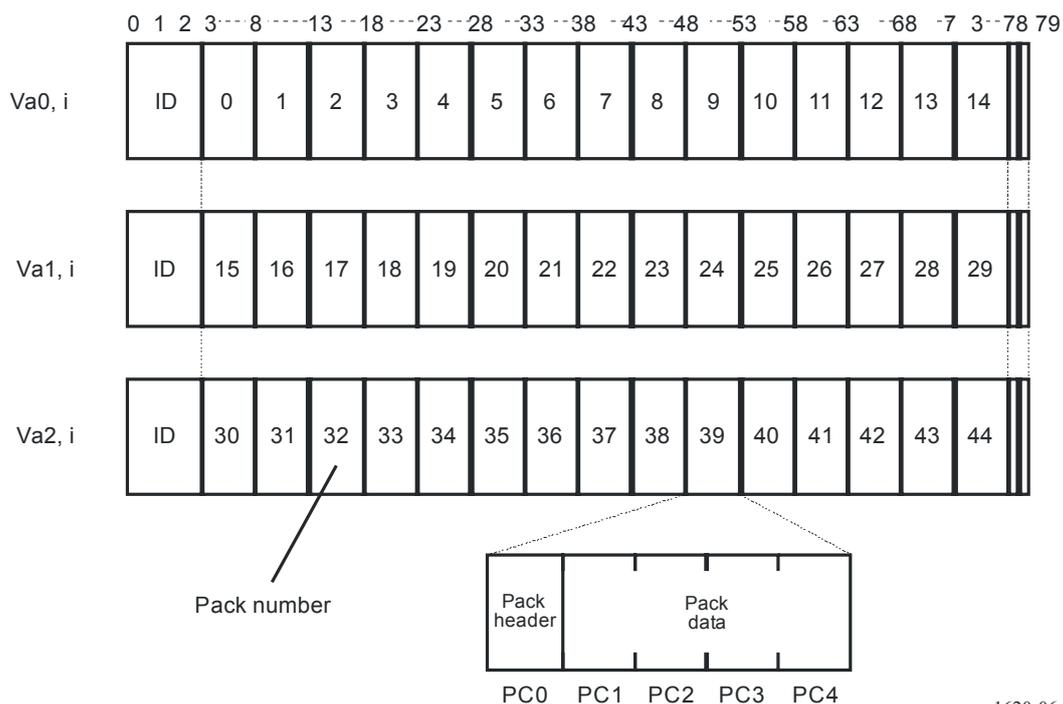**Data in the VAUX section**

Byte position number

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Table 13 shows the mapping of the VAUX packs of the VAUX DIF blocks. One VAUX source pack (VS) and one VAUX source control pack (VSC) shall exist in each frame. The remaining VAUX packs of the DIF blocks in a DIF sequence are reserved and the value of all reserved words shall be set to FF$_h$.

If VAUX data are not transmitted, a NO INFO pack, which is filled with FF$_h$, shall be transmitted.

TABLE 13

Mapping of VAUX pack in a DIF sequence

Pack	number	Pack data
Even DIF sequence	Odd DIF sequence	
39	0	VS
40	1	VSC

Even DIF sequence:
DIF sequence number 0, 2, 4, 6, 8 for 60-Hz system
DIF sequence number 0, 2, 4, 6, 8, 10 for 50-Hz system
Odd DIF sequence:
DIF sequence number 1, 3, 5, 7, 9 for 60-Hz system
DIF sequence number 1, 3, 5, 7, 9, 11 for 50-Hz system.

3.5.2.1   VAUX source pack (VS)

Table 14 shows the structure of the VAUX source pack.

TABLE 14

Structure of VAUX source pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	Res	Res	Res	Res	Res	Res	Res	Res
PC3	Res	Res	50/60	STYPE				
PC4	0	Res	Res	Res	Res	Res	Res	Res

50/60:
0 = 60-Hz system
1 = 50-Hz system

STYPE: Video signal type

For 60-Hz system
1 0 1 0 0 b = 1 920 × 1 080/60/I – 100 Mb/s compression
1 0 1 0 1 b = Reserved
1 1 0 0 0 b = 1 280 × 720/60/P – 100 Mb/s compression
Other = Reserved

For 50-Hz system
1 0 1 0 0 b = 1 920 × 1 080/50/I – 100 Mb/s compression
1 1 0 0 0 b = 1 280 × 720/50/P – 100 Mb/s compression
Other Values = Reserved
Res: Reserved bit for future use
Default value shall be set to 1.

3.5.2.2   VAUX source control pack

Table 15 shows the structure of the VAUX source control pack.

TABLE 15

Structure of VAUX source control pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	Res	Res
PC2	Res	Res	0	0	Res	DISP		
PC3	FF	FS	FC	Res	Res	Res	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system
    0 0 b = Copy free
    Other = Reserved

DISP: Display select mode
    0 1 0 b = 16:9
    Other = Reserved

FF: Frame/field flag
    For the 1 920 × 1 080-line system (see Table 16)
      FF indicates whether two consecutive fields are delivered, or one field is repeated
      twice during one video frame period (see Table 16)
    0 = Only one of the two fields is delivered twice
    1 = Both fields are delivered in order.
    For the 1 280 × 720-line system (see Table 17)
      FF indicates whether two consecutive video frames are delivered, or one video frame is
      repeated twice during the two video frames period.
    0 = Only one of the two video frames is delivered twice.
    1 = Both video frames are delivered in order.

FS: First/second field flag
    For the 1 920 × 1 080-line system (see Table 16)
      FS indicates a field which is delivered during the field one period (see Table 16)
    0 = Field 2 is delivered
    1 = Field 1 is delivered.
    For the 1 280 × 720-line system (see Table 17)
      FS indicates a video frame which is delivered during the video frame one period.
    0 = Video frame 2 is delivered.
    1 = Video frame 1 is delivered.

TABLE 16

FF/FS for the 1 920 × 1 080-line system

FF	FS	Output field
1	1	Field 1 and field 2 are output in this order (1,2 sequence).
1	0	Field 2 and field 1 are output in this order (2,1 sequence).
0	1	Field 1 is output twice.
0	0	Field 2 is output twice.

TABLE 17

FF/FS for the 1 280 × 720-line system

FF	FS	Output video frame
1	1	Video frame 1 and video frame 2 are output in this order (1, 2 sequence).
1	0	Video frame 2 and video frame 1 are output in this order (2, 1 sequence).
0	1	Video frame 1 is output twice.
0	0	Video frame 2 is output twice.

FC: Frame change flag

   For the 1 920 × 1 080-line system

   FC indicates whether the picture of the current video frame is repeated based on the immediate previous video frame.

   0 = Same picture as the previous video frame

   1 = Different picture than the previous video frame

   For the 1 280 × 720-line system

   FC indicates whether the picture of the current two video frames is repeated based on the immediate previous two video frames.

   0 = Same picture as the previous two video frames

   1 = Different picture than the previous two video frames

Res: Reserved bit for future use

   Default value shall be set to 1.

3.6 Audio section

3.6.1 ID

The ID part of each DIF block in the audio section shall be the same as described in § 3.3.1. The section type shall be 011.

3.6.2 Data

The data part (payload) of each DIF block in the audio section is shown in Fig. 7. The data of the DIF block in the audio section shall be composed of 5 bytes of audio auxiliary data (AAUX) and 72 bytes of audio data which is encoded and shuffled by the process as described in § 3.6.2.1 and § 3.6.2.2.

FIGURE 7

Data in the audio section
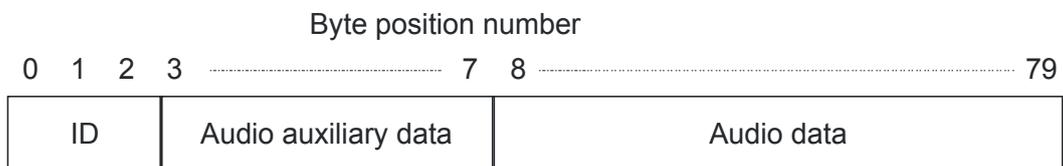
1620-07

3.6.2.1 Audio encoding

3.6.2.1.1 Source coding

Each audio input signal shall be sampled at 48 kHz, with 16-bit quantization. The system provides eight audio channels. Audio data for each audio channel are located in each respective audio block.

3.6.2.1.2 Emphasis

The audio encoding shall be carried out with the first order pre-emphasis of 50/15 µs. For analogue input recording, emphasis shall be off – the default state.

3.6.2.1.3 Audio error code

In the encoded audio data, 8000_h shall be assigned as the audio error code to indicate an invalid audio sample. This code corresponds to the negative full scale value in ordinary twos complement representation. When the encoded data includes 8000_h, it shall be converted to 8001_h.

3.6.2.1.4 Relative audio-video timing

1 920 × 1 080-line system

An audio frame shall begin with an audio sample acquired within the duration of minus 50 samples relative to zero samples from the start of line number 1.

1 280 × 720-line system

An audio frame shall begin with an audio sample acquired within the duration of minus 50 samples relative to zero samples from the start of line number 1 of video frame 1.

3.6.2.1.5   Audio frame processing

The audio data shall be processed in each audio frame. Each audio frame shall contain 1 602 or 1 600 audio samples for the 60-Hz system or 1 920 audio samples for the 50-Hz system for an audio channel with associated status, user, and validity data. For the 60-Hz system, the number of audio samples per audio frame shall follow the five-frame sequence as shown below:

> 1 600, 1 602, 1 602, 1 602, 1 602 samples.

One audio frame shall be capable of 1 620 samples for the 60-Hz system or 1 944 samples for the 50-Hz system. The unused space at the end of each audio frame is filled with arbitrary values.

3.6.2.2   Audio shuffling

The 16-bit audio data word shall be divided into two bytes. The upper byte shall contain MSB, and the lower byte shall contain LSB, as shown in Fig. 8. Audio data shall be shuffled over DIF sequences and DIF blocks within an audio frame. The data bytes are defined as D_n (n = 0, 1, 2, ...) which is sampled in the n-th order within an audio frame and shuffled by each D_n unit.

The data shall be shuffled through the process as expressed by the following equations:
60-Hz system –

    DIF channel number: i = 0: Audio CH1,CH2
                          i = 1: Audio CH3,CH4
                          i = 2: Audio CH5,CH6
                          i = 3: Audio CH7,CH8
    DIF Sequence number: (INT (n/3) + 2 x (n mod 3)) mod 5 for Audio CH1,CH3,CH5,CH7
                          (INT (n/3) + 2 x (n mod 3)) mod 5 + 5 for Audio CH2,CH4,CH6,CH8
    Audio DIF block number: 3 x (n mod 3) + INT ((n mod 45) / 15)
    byte position number: 8 + 2 x INT(n/45) for the most significant byte
                              9 + 2 x INT(n/45) for the least significant byte
            where   n = 0 to 1 619

50-Hz system –

    DIF channel number: i = 0: Audio CH1,CH2
                          i = 1: Audio CH3,CH4
                          i = 2: Audio CH5,CH6
                          i = 3: Audio CH7,CH8
    DIF Sequence number: (INT (n/3) + 2 x (n mod 3)) mod 6 for Audio CH1,CH3,CH5,CH7
                          (INT (n/3) + 2 x (n mod 3)) mod 6 + 6 for Audio CH2,CH4,CH6,CH8
    Audio DIF block number: 3 x (n mod 3) + INT ((n mod 54) / 18)
    byte position number: 8 + 2 x INT(n/54) for the most significant byte
                              9 + 2 x INT(n/54) for the least significant byte
            where   n = 0 to 1 943

FIGURE 8

Conversion of audio sample to audio data bytes
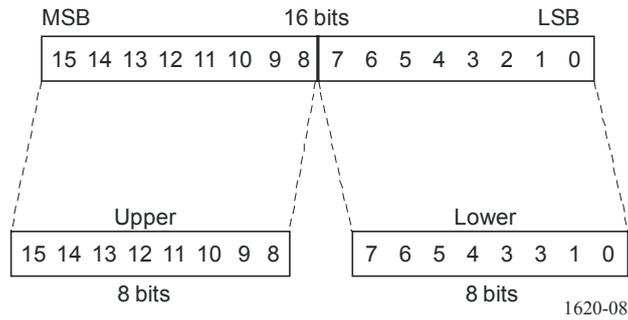
3.6.2.3   **Audio auxiliary data (AAUX)**

AAUX shall be added to the shuffled audio data as shown in Figs 7 and 9. The AAUX pack shall include the AAUX pack header and data (AAUX payload). The length of the AAUX pack shall be 5 bytes as shown in Fig. 9, which depicts the AAUX pack arrangement. The audio packs are numbered 0 to 8 as shown in Fig. 9. This number is called an audio pack number.

Table 18 shows the structure of the AAUX pack. One AAUX source pack (AS) and one AAUX source control pack (ASC) shall be included in the compressed stream.

FIGURE 9

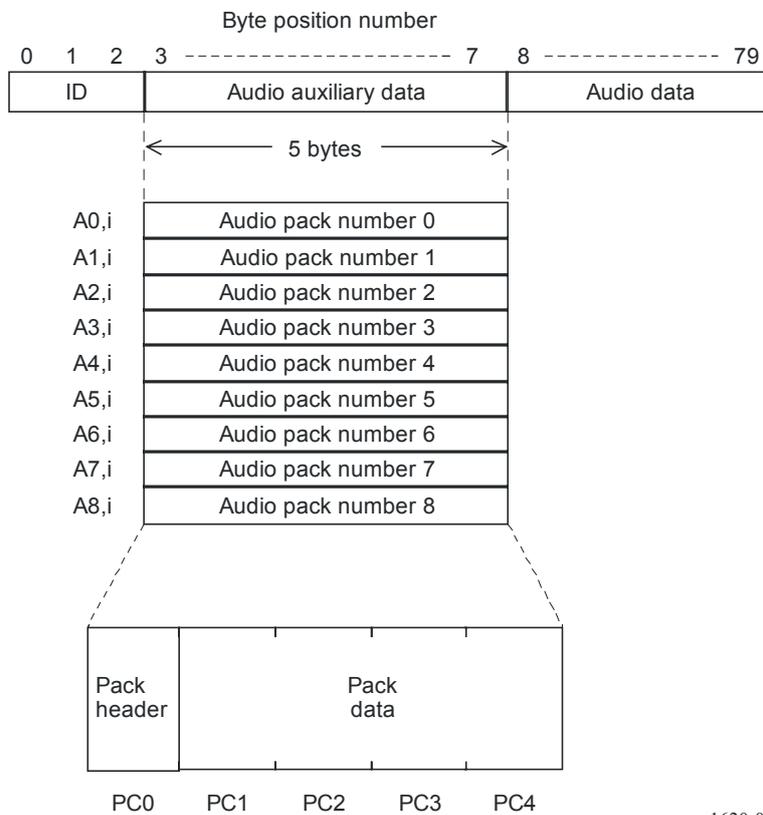**Arrangement of AAUX packs in audio auxiliary data**

TABLE 18

Mapping of AAUX pack in a DIF sequence

Audio pack	number	
Even DIF sequence	Odd DIF sequence	Pack data
3	0	AS
4	1	ASC

Even DIF sequence:
  DIF sequence number 0, 2, 4, 6, 8 for 60-Hz system
  DIF sequence number 0, 2, 4, 6, 8, 10 for 50-Hz system
Odd DIF sequence:
  DIF sequence number 1, 3, 5, 7, 9 for 60-Hz system
  DIF sequence number 1, 3, 5, 7, 9, 11 for 50-Hz system.

3.6.2.3.1 AAUX source pack (AS)

The AAUX source pack shall be configured as shown in Table 19.

TABLE 19

Structure of AAUX source pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	Res	AF SIZE					
PC2	0	CHN		Res	AUDIO MODE			
PC3	Res	Res	50/60	STYPE				
PC4	Res	Res	SMP			QU		

LF: Locked mode flag
    Locking condition of audio sampling frequency with video signal.
    0 = Locked mode
    1 = Reserved

AF SIZE: The number of audio samples per frame
    0 1 0 1 0 0 b = 1 600 samples / frame (60-Hz system)
    0 1 0 1 1 0 b = 1 602 samples / frame (60-Hz system)
    0 1 1 0 0 0 b = 1 920 samples / frame (50-Hz system)
    Other = Reserved

CHN: The number of audio channels within an audio block
    0 0 b = One audio channel per an audio block
    Other = Reserved
    An audio block consists of 45 DIF blocks (9 DIF blocks x 5 DIF sequences) for the 60-Hz system and 54 DIF blocks (9 DIF blocks x 6 DIF sequences) for the 50-Hz system.

AUDIO MODE: The contents of the audio signal on each audio channel
    0 0 0 0   b = Audio CH1,CH3,CH5,CH7
    0 0 0 1   b = Audio CH2,CH4,CH6,CH8
    1 1 1 1   b = Invalid audio data
    Other = Reserved

50/60:
    0 = 60-Hz system
    1 = 50-Hz system

STYPE: Audio blocks for each frame
  0 0 0 1 1 b = 8 audio blocks
  Other = Reserved

SMP: Sampling frequency
  0 0 0 b = 48 kHz
  Other = Reserved

QU: Quantization
  0 0 0 b = 16 bits linear
  Other = Reserved

Res: Reserved bit for future use
  Default value shall be set to 1.

3.6.2.3.2 AAUX source control pack (ASC)

The AAUX source control pack shall be configured as shown in Table 20.

TABLE 20

Structure of AAUX source control pack

MSB   LSB

PC0	0	1	0	1	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	EFC	
PC2	REC ST	REC END	FADE ST	FADE END	Res	Res	Res	Res
PC3	DRF	SPEED						
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system
  0 0 b = Copy free
  Other = Reserved

EFC: Emphasis audio channel flag
  0 0 b = Emphasis off
  0 1 b = Emphasis on
  Other = Reserved
  EFC shall be set for each audio block.

REC ST: Recording start point
  0 = Recording start point
  1 = Not recording start point
 At the recording start frame, REC ST is set to zero for duration of one audio block which is equal to
 5 or 6 DIF sequences for each audio channel.

REC END: Recording end point
  0 = Recording end point
  1 = Not recording end point

At the recording end frame, REC END is set to zero for duration of one audio block which is equal
to 5 or 6 DIF sequences for each audio channel.

FADE ST: Fading of recording start point
  0 = Fading off
  1 = Fading on

The FADE ST information is only effective at the recording start frame (REC ST = 0).If FADE ST is 1 at the recording start frame, the output audio signal should be faded in from the first sampling signal of the frame. If FADE ST is 0 at the recording start frame, the output audio signal should not be faded.

FADE END: Fading of recording end point
        0 = Fading off
        1 = Fading on
        The FADE END information is only effective at the recording end frame (REC END = 0). If FADE END is 1 at the recording end frame, the output audio signal should be faded out to the last sampling signal of the frame. If FADE END is 0 at the recording end frame, the output audio signal should not be faded.

DRF: Direction flag
     0 = Reverse direction
     1 = Forward direction

SPEED: VTR Shuttle speed (see Table 21)

TABLE 21

SPEED code definition

Codeword MSB LSB	Shuttle speed of VTR	
	60-Hz system	50-Hz system
0000000	0/120 (=0)	0/100 (=0)
0000001	1/120	1/100
:	:	:
1100100	100/120	100/100 (=1)
:	:	Reserved
1111000	120/120 (=1)	Reserved
:	Reserved	Reserved
1111110	Reserved	Reserved
1111111	Data invalid	Data invalid

Res: Reserved bit for future use
    Default value shall be set to 1.

3.7   Video section

3.7.1   ID

The ID part of each DIF block in the video section shall be the same as described in § 3.3.1. The section type shall be 100.

3.7.2 Data

Data part (payload) of each DIF block in the video section consists of 77 bytes of video data which shall be sampled, shuffled and encoded. The video data of every frame shall be processed as described in clause 4. This 77 byte data are called a compressed macro block.

3.7.2.1   DIF block and compressed macro block

Correspondence between Video DIF blocks and video compressed macro blocks CM h,i,j,k is shown in Table 22 for the 60-Hz system, Table 23 for the 1 920 × 1 080/50/I system and Table 24 for the 1 280 × 720/50/P system.

The rule defining the correspondence between video DIF blocks and compressed macro blocks is as shown below:

60-Hz and 1 280 × 720/50/P systems –
```
for(h=0; h<4; h++){
   for(s=0; s<2; s++){
      for(k=0; k<27; k++){
         for(t=0; t<5; t++){
               a = (4h + s + 2t + 2) mod 10;
               b = (4h + s + 2t + 6) mod 10;
               c = (4h + s + 2t + 8) mod 10;
               d = (4h + s + 2t + 0) mod 10;
               e = (4h + s + 2t + 4) mod 10;
               DBNq = (5t + 25k) mod 135;
               DSNp = INT((5t + 25k + 675s) / 135);

               V DBNq, h of DSNp = CM h,a,2,k
               V (DBNq + 1), h of DSNp = CM h,b,1,k
               V (DBNq + 2), h of DSNp = CM h,c,3,k
               V (DBNq + 3), h of DSNp = CM h,d,0,k
               V (DBNq + 4), h of DSNp = CM h,e,4,k
         }
      }
   }
}
```

where
        DBNq: DIF block number
        DSNp: DIF sequence number
        h: Divided block
        s, t: Vertical order of super block
        k: Macro block order in super block

1 920 × 1 080/50/I system –

```
for(h=0; h<4; h++){
   for(k=0; k<27; k++){
      for(i=0; i<11; i++){
            a = (4h + i + 2) mod 11;
            b = (4h + i + 6) mod 11;
            c = (4h + i + 8) mod 11;
            d = (4h + i + 0) mod 11;
            e = (4h + i + 4) mod 11;
            DBNq = (5i + 55k) mod 135;
            DSNp = INT((5i + 55k) / 135);

            V DBNq, h of DSNp = CM h,a,2,k
            V (DBNq + 1), h of DSNp = CM h,b,1,k
            V (DBNq + 2), h of DSNp = CM h,c,3,k
            V (DBNq + 3), h of DSNp = CM h,d,0,k
            V (DBNq + 4), h of DSNp = CM h,e,4,k
      }
   }
}
for(k=0; k<27; k++){
            DBNq = 5k;
            DSNp = 11;

            V DBNq, 0 of DSNp = CM 0,11,0,k
            V (DBNq + 1), 0 of DSNp = CM 0,11,1,k
            V (DBNq + 2), 0 of DSNp = CM 0,11,2,k
```

        V (DBNq + 3), 0 of DSNp = CM 0,11,3,k
        V (DBNq + 4), 0 of DSNp = CM 0,11,4,k
}
where

        DBNq: DIF block number
        DSNp: DIF sequence number
        h: Divided block
        i: Vertical order of super block
        k: Macro block order in super block

TABLE 22

Video DIF blocks and compressed macro blocks for the 60-Hz system

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	9	:	:
		V 134,0	CM 0,3,4,26
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,0,1,0
		V 2,1	CM 1,2,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	9	:	:
		V 134,1	CM 1,7,4,26
:	:	:	:
3	0	V 0,3	CM 3,4,2,0
		V 1,3	CM 3,8,1,0
		V 2,3	CM 3,0,3,0
		V 3,3	CM 3,2,0,0
		V 4,3	CM 3,6,4,0
		:	:
	:	:	:
	9	:	:
		V 134,3	CM 3,5,4,26

TABLE 23

**Video DIF blocks and compressed macro blocks
for the 1 920 × 1 080/50/I system**

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	10	:	:
		V 134,0	CM 0,3,4,26
	11	V 0,0	CM 0,11,0,0
		V 1,0	CM 0,11,1,0
		:	:
		V 134,0	CM 0,11,4,26
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,10,1,0
		V 2,1	CM 1,1,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	10	:	:
		V 134,1	CM 1,7,4,26
	11	V 0,1	—
		:	:
		V 134,1	—
:	:	:	:
3	0	V 0,3	CM 3,3,2,0
		V 1,3	CM 3,7,1,0
		V 2,3	CM 3,9,3,0
		V 3,3	CM 3,1,0,0
		V 4,3	CM 3,5,4,0
		:	:
	:	:	:
	10	:	:
		V 134,3	CM 3,4,4,26
	11	V 0,3	—
		:	:
		V 134,3	—

TABLE 24

**Video DIF blocks and compressed macro blocks
for the 1 280 × 720/50/P system**

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	9	:	:
		V 134,0	CM 0,3,4,26
	10	V 0,0	—
		:	:
		V 134,0	—
	11	V 0,0	—
		:	:
		V 134,0	—
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,0,1,0
		V 2,1	CM 1,2,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	9	:	:
		V 134,1	CM 1,7,4,26
	10	V 0,1	—
		:	:
		V 134,1	—
	11	V 0,1	—
		:	:
		V 134,1	—
:	:	:	:
3	0	V 0,3	CM 3,4,2,0
		V 1,3	CM 3,8,1,0
		V 2,3	CM 3,0,3,0
		V 3,3	CM 3,2,0,0
		V 4,3	CM 3,6,4,0
		:	:
	:	:	:
	9	:	:
		V 134,3	CM 3,5,4,26
	10	V 0,3	—
		:	:
		V 134,3	—
	11	V 0,3	—
		:	:
		V 134,3	—

4 Video compression

This section includes the video compression processing for the 1 920 × 1 080/60/I system, the 1 920 × 1 080/50/I system, the 1 280 × 720/60/P system and the 1 280 × 720/50/P system.

4.1 Video structure

4.1.1 Video sampling structure

The video sampling structure shall comply with Recommendation ITU-R BT.709 for 1 920 × 1 080-line systems, and Recommendations ITU-R BT.1543 and ITU-R BT.1847 for the 1 280 × 720-line systems. The construction of luminance (Y) and two colour-difference signals (C_R, C_B) is described in Table 25. A sample conversion from 10-bit input video to 8 bits or more is provided by the resampling process (the first processing block of Fig. 1).

4.1.1.1 Video frame pixel structure

1 920 × 1 080/60/I system

1 920 pixels of luminance and 960 pixels of each colour-difference signal per line shall be transmitted as shown in Fig. 10. The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (−508 to 507) by inverting the MSB of the input video signal.

1 920 × 1 080/50/I system

1 920 pixels of luminance and 960 pixels of each colour-difference signal per line shall be transmitted as shown in Fig. 11. The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (−508 to 507) by inverting the MSB of the input video signal.

1 280 × 720/60/P system

1 280 pixels of luminance and 640 pixels of each colour-difference signal per line shall be transmitted as shown in Fig. 12. The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (−508 to 507) by inverting the MSB of the input video signal.

1 280 × 720/50/P system

1 280 pixels of luminance and 640 pixels of each colour-difference signal per line shall be transmitted as shown in Fig. 12. The sampling starting point in the active period of the C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (−508 to 507) by inverting the MSB of the input video signal.

4.1.1.2 Video frame line structure

1 920 × 1 080 line system

540 lines for Y, C_R, and C_B signals from each field shall be transmitted. The transmitted lines in each two fields are shown in Table 25.

1 280 × 720 line system

720 lines for Y, C_R and C_B signals from each video frame shall be transmitted. The transmitted lines in each video frame are shown in Table 25.

4.1.1.3   Horizontal resampling

1 920 × 1 080/60/I system

1 920 horizontally sampled Y signals shall be resampled to 1 280 pixels. The 960 horizontally sampled C_R and C_B signals shall be resampled to 640 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more. (See Annex 2.)

1 920 × 1 080/50/I system

1 920 horizontally sampled Y signals shall be resampled to 1 440 pixels. The 960 horizontally sampled C_R and C_B signals shall be resampled to 720 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more. (See Annex 2.)

1 280 × 720/60/P and 1 280 × 720/50/P systems

The 1 280 horizontally sampled Y signals shall be resampled to 960 pixels. The 640 horizontally sampled C_R and C_B signals shall be resampled to 480 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more. (See Annex 2.)

TABLE 25

Source video parameters

		1 920 × 1 080/60/I system	1 920 × 1 080/50/I system	1 280 × 720/60/P system	1 280 × 720/50/P system
Sampling frequency	Y	74.25 / 1.001 MHz	74.25 MHz	74.25 / 1.001 MHz	74.25 MHz
	C_R, C_B	37.125 / 1.001 MHz	37.125 MHz	37.125 / 1.001 MHz	37.125 MHz
Total number of pixels per line	Y	2 200	2 640	1 650	1 980
	C_R, C_B	1 100	1 320	825	990
The number of active pixels per line	Y	1 920		1 280	
	C_R, C_B	960		640	
Total number of lines per video frame		1 125		750	
The number of active lines per video frame		1 080		720	
The active line numbers		Field 1 21 to 560		26 to 745	
		Field 2 584 to 1 123			
Quantization		Each sample is linearly quantized to 10 bits for Y, C_R and C_B.			
The relation between video signal level and quantized level	Scale	4 to 1 019			
	Y	Video signal level of white: 940 / Video signal level of black: 64		Quantized level 877	
	C_R, C_B	Video signal level of gray: 512		Quantized level 897	

FIGURE 10

Sampling structure for the 1 920 × 1 080/60/I system

1620-10
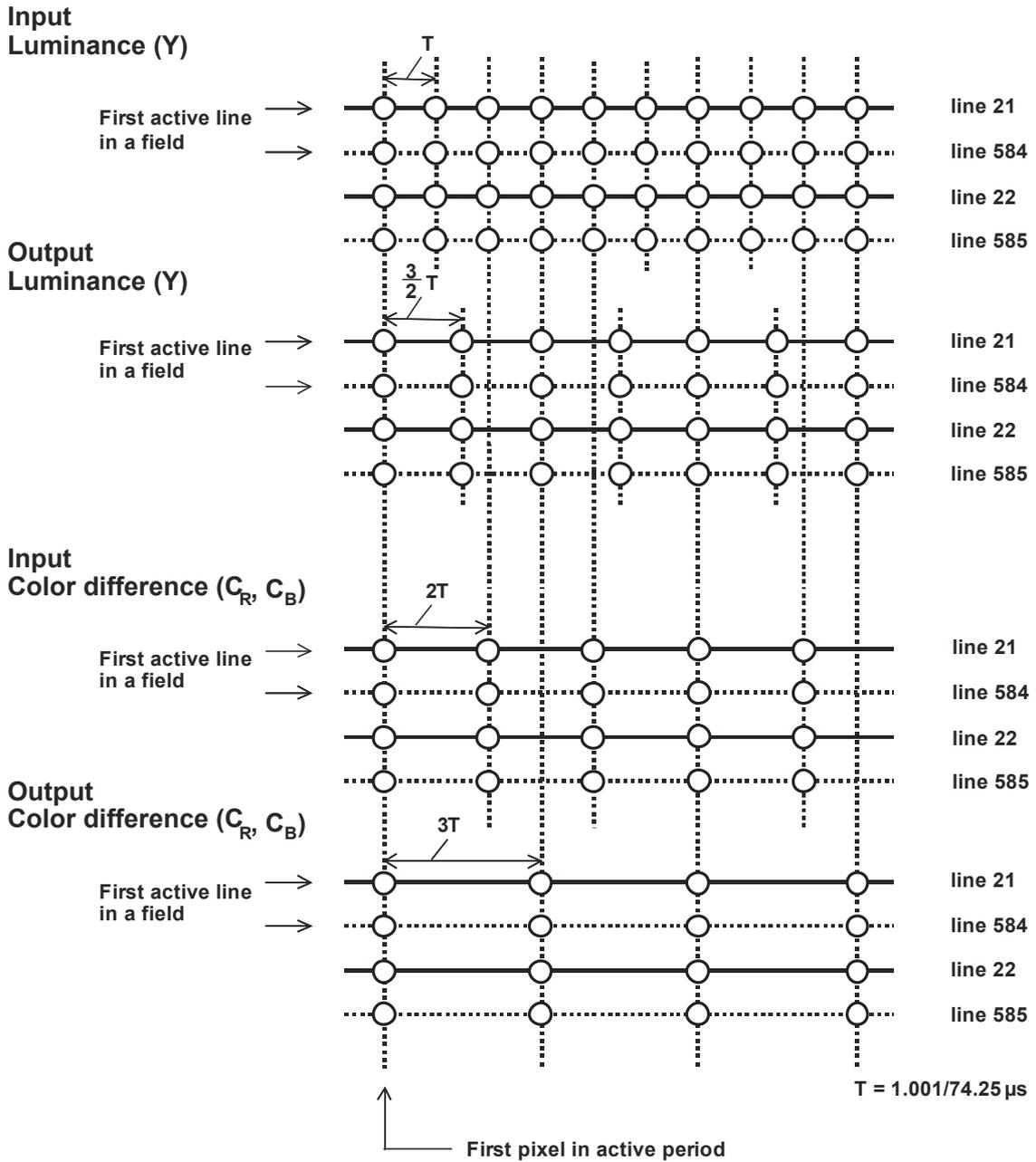
FIGURE 11

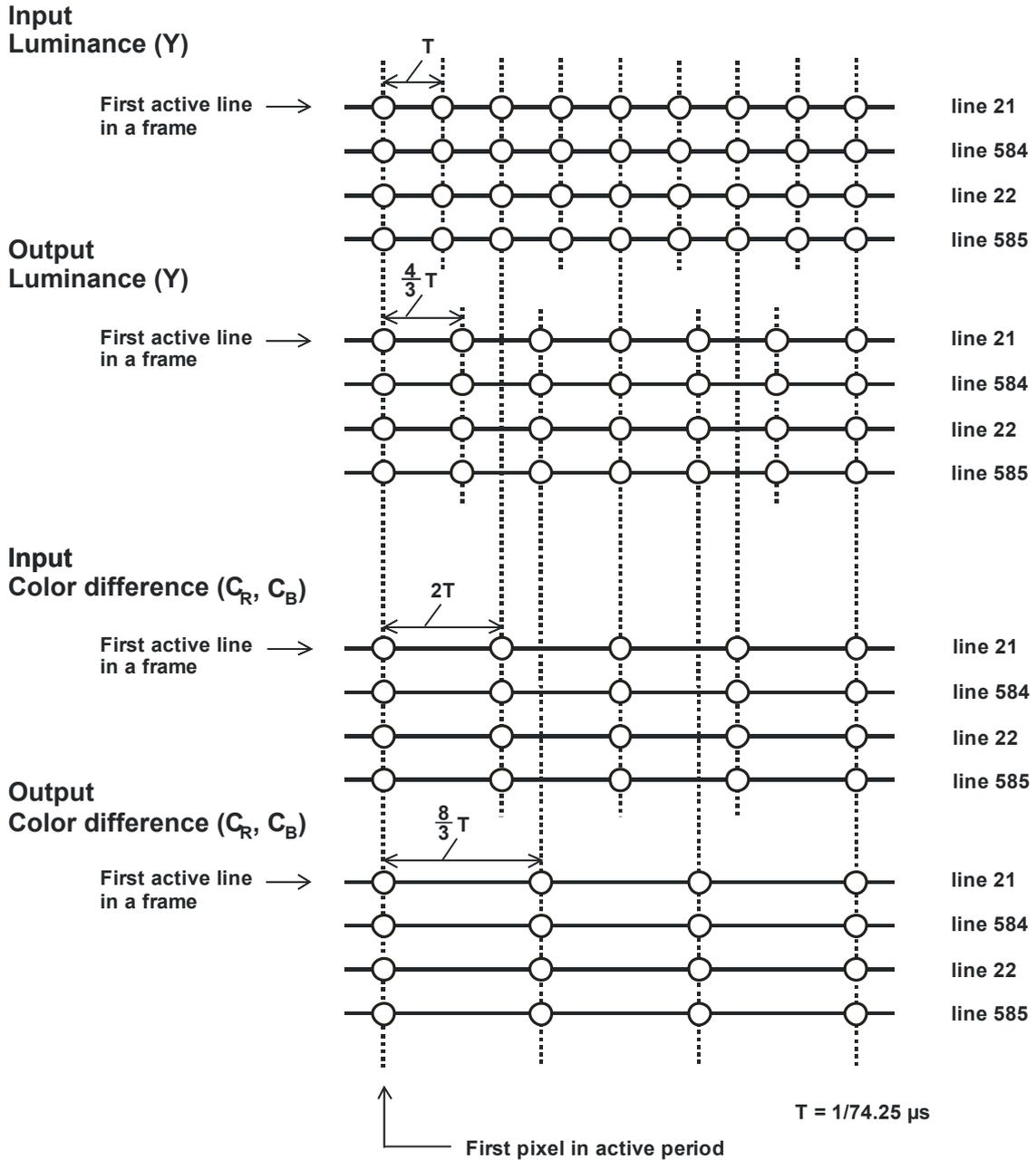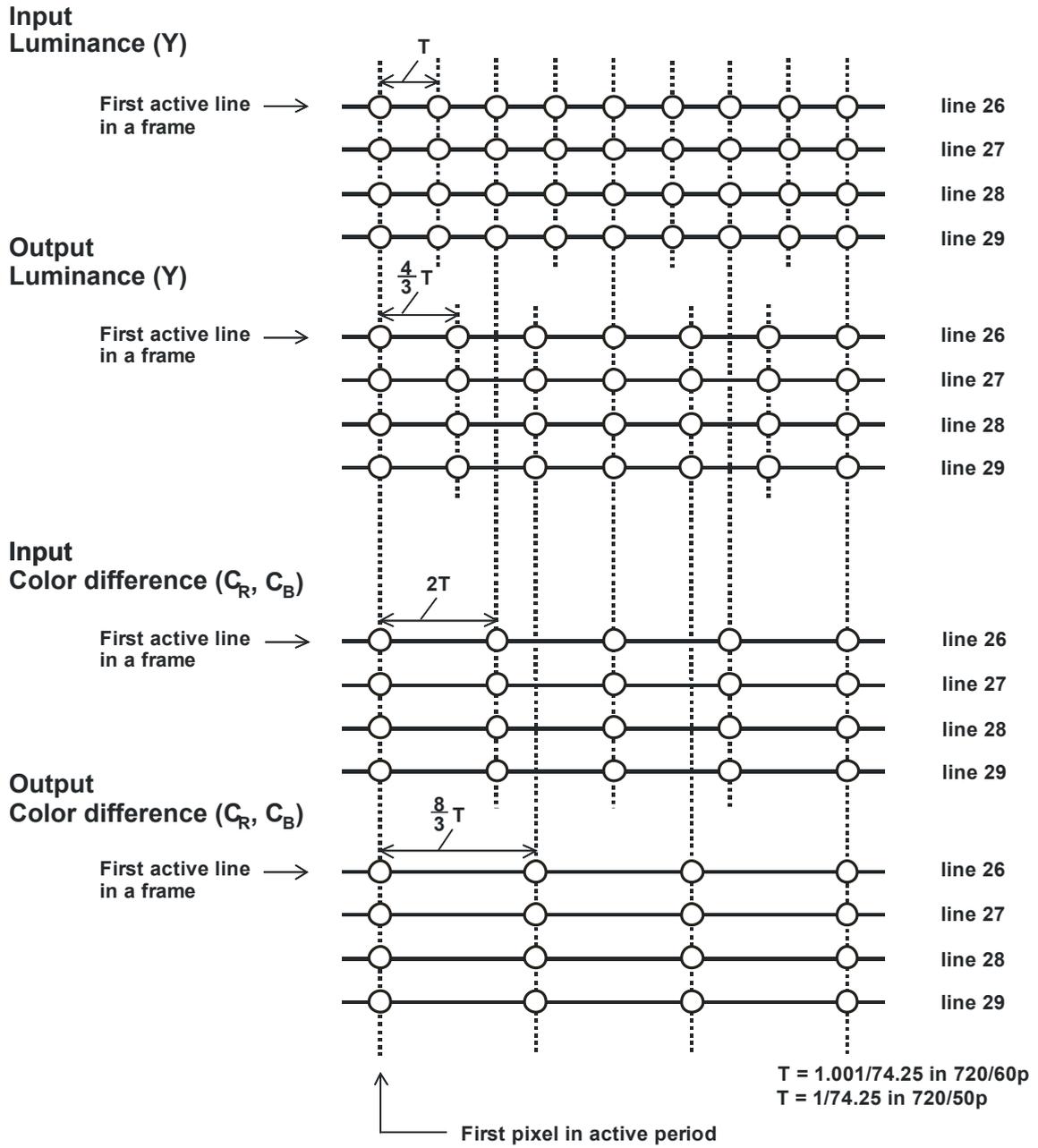**Sampling structure for the 1 920 × 1 080/50/I system**

T = 1/74.25 μs

First pixel in active period

1620-11

FIGURE 12

Sampling structure for the 720/60/P and 720/50/P systems

T = 1.001/74.25 in 720/60p
T = 1/74.25 in 720/50p

1620-12

4.1.2   DCT block

The Y, C_R, and C_B pixels in each video frame shall be divided into DCT blocks as shown in Fig. 13 for the 1 920 × 1 080-line system, and Fig. 14 for the 1 280 × 720-line system. The DCT blocks shall be structured with a rectangular area of eight vertical pixels and eight horizontal pixels in a video frame. The value of x shows the horizontal coordinate from the left and the value of y shows the vertical coordinate from the top. For the 1 920 × 1 080-line system, even lines of y = 0, 2, 4, 6 are the horizontal lines of field one, and odd lines of y = 1, 3, 5, 7 are those of field two.

DCT block arrangement in each video frame

1 920 × 1 080/60/I system

The arrangement of horizontal DCT blocks in each video frame shall be as shown in Fig. 15. The same horizontal arrangement is repeated to 135 DCT blocks in the vertical direction. Pixels in one video frame are divided into 43 200 DCT blocks.

   Y: 135 vertical DCT blocks × 160 horizontal DCT blocks = 21 600 DCT blocks

   C_R: 135 vertical DCT blocks × 80 horizontal DCT blocks = 10 800 DCT blocks

   C_B: 135 vertical DCT blocks × 80 horizontal DCT blocks = 10 800 DCT blocks.

1 920 × 1 080/50/I system

The arrangement of horizontal DCT blocks in each video frame shall be as shown in Fig. 16. The same horizontal arrangement is repeated to 135 DCT blocks in the vertical direction. Pixels in one video frame are divided into 48 600 DCT blocks.

   Y: 135 vertical DCT blocks × 180 horizontal DCT blocks = 24 300 DCT blocks

   C_R: 135 vertical DCT blocks × 90 horizontal DCT blocks = 12 150 DCT blocks

   C_B: 135 vertical DCT blocks × 90 horizontal DCT blocks = 12 150 DCT blocks.

1 280 × 720/60/P and 1 280 × 720/50/P systems

The arrangement of horizontal DCT blocks in each video frame shall be as shown in Fig. 17. The same horizontal arrangement is repeated to 90 DCT blocks in the vertical direction. Pixels in one video frame are divided into 21 600 DCT blocks.

   Y: 90 vertical DCT blocks × 120 horizontal DCT blocks = 10 800 DCT blocks

   C_R: 90 vertical DCT blocks × 60 horizontal DCT blocks =   5 400 DCT blocks

   C_B: 90 vertical DCT blocks × 60 horizontal DCT blocks =   5 400 DCT blocks.

4.1.3   Macro block

Each macro block shall consist of eight DCT blocks. Figure 18 for the 1 920 × 1 080-line systems and Fig. 19 for the 1 280 × 720-line systems .

4.1.3.1   Arrangement of macro block

1 920 × 1 080/60/I system

Macro block arrangement in each video frame shall have the following two steps.

Step 1: Arranging macro blocks

Pixels in each video frame shall be divided into 5 400 macro blocks as shown in Fig. 20.

Each macro block except the bottom macro blocks shall consist of four DCT blocks of Y which are horizontally and vertically adjacent, two vertically adjacent DCT blocks of C_R and two vertically adjacent DCT blocks of C_B;

where, 67 vertical macro blocks × 80 horizontal macro blocks = 5 360 macro blocks.

Each bottom macro block shall consist of four horizontally adjacent DCT blocks of Y, two horizontally adjacent DCT blocks of C_R and two horizontally adjacent DCT blocks of C_B;

where, 1 vertical macro blocks × 40 horizontal macro blocks = 40 macro blocks.

Step 2: Rearranging macro blocks

Sets consisting of 40 macro blocks which are named A0 to A7 and sets consisting of 30 macro blocks which are named A8 to A15 shall be arranged as shown in Fig. 20.

40 macro blocks in A16 shall be arranged into 4 vertical macro blocks × 10 horizontal macro blocks in B16 respectively as shown in Fig. 20;

where, 60 vertical macro blocks × 90 horizontal macro blocks = 5 400 macro blocks.

1 920 × 1 080/50/I system

Macro block arrangement in each video frame shall have the following two steps.

Step 1: Arranging macro blocks

Pixels in each video frame shall be divided into 6 075 macro blocks as shown in Fig. 21.

Each macro block except the bottom macro blocks shall consist of four DCT blocks of Y which are horizontally and vertically adjacent, two vertically adjacent DCT blocks of C_R and two vertically adjacent DCT blocks of C_B;

where, 67 vertical macro blocks × 90 horizontal macro blocks = 6 030 macro blocks.

Each bottom macro block shall consist of four horizontally adjacent DCT blocks of Y, two horizontally adjacent DCT blocks of C_R and two horizontally adjacent DCT blocks of C_B;

where, 1 vertical macro blocks × 45 horizontal macro blocks = 45 macro blocks.

Step 2: Rearranging macro blocks

The macro blocks shall be divided into a main unit and an edge unit. The edge unit shall contain the top macro blocks in A0 and the bottom macro blocks in A1 as shown in Fig. 21. The main unit shall contain the remaining blocks;

where,

main unit: 66 vertical macro blocks × 90 horizontal macro blocks = 5 940 macro blocks.

edge unit: 1 vertical macro blocks × 135 horizontal macro blocks = 135 macro blocks.

1 280 × 720/60/P and 1 280 × 720/50/P systems

Pixels in each video frame shall be divided into 2 700 macro blocks as shown in Fig. 22;

where, 45 vertical macro blocks × 60 horizontal macro blocks = 2 700 macro blocks.

4.1.3.2 Divided blocks

1 920 × 1 080/60/I system

The macro blocks in each video frame shall be divided into the halfway blocks as shown in Fig. 23. Each halfway block H consists of nine macro blocks horizontally and one macro block vertically.

The halfway blocks H shall be distributed into the divided blocks as follows:

Divided blocks:　　h=0 : H 2m,2n

　　　　　　　　　h=1 : H 2m,2n+1

　　　　　　　　　h=2 : H 2m+1,2n

　　　　　　　　　h=3 : H 2m+1,2n+1

　　　　　　　where,　m = 0, 1 ,2, ..., 29

　　　　　　　　　　　　n = 0, 1, 2, 3, 4.

As a result, one video frame is divided into four divided blocks. Each divided block consists of 30 vertical macro blocks × 45 horizontal macro blocks.

1 920 × 1 080/50/I system

The macro blocks in the main unit shall be divided into the halfway blocks as shown in Fig. 24. Each halfway block H consists of nine horizontally adjacent macro blocks.

The halfway blocks H shall be distributed into the divided blocks as follows:

Divided blocks:　　h=0 : H 2m,2n

　　　　　　　　　h=1 : H 2m,2n+1

　　　　　　　　　h=2 : H 2m+1,2n

　　　　　　　　　h=3 : H 2m+1,2n+1

　　　　　　　where,　m = 0, 1, 2, ..., 32

　　　　　　　　　　　　n = 0, 1, 2, 3, 4.

As a result, the main unit is divided into four divided blocks. Each divided block is consists of 33 vertical macro blocks × 45 horizontal macro blocks.

1 280 × 720/60/P and 1 280 × 720/50/P systems

The macro blocks in each video frame shall be divided into the halfway blocks as shown in Fig. 25. Each halfway block H consists of six macro blocks horizontally and one macro block vertically.

The halfway blocks H shall be distributed into the divided blocks as follows below:

Divided blocks:　　h=0 : H m, 2n

　　　　　　　　　h=1 : H m, 2n+1

　　　　　　　　　h=2 : H m+45, 2n

　　　　　　　　　h=3 : H m+45, 2n+1

　　　　　　　where,　m = 0, 1, 2, ..., 44

　　　　　　　　　　　　n = 0, 1, 2, 3, 4.

As a result, each two video frames are divided into four divided blocks. Each divided block is consists of 45 vertical macro blocks × 30 horizontal macro blocks.

FIGURE 13

DCT block and the pixel coordinates for the 1 920 × 1 080-line system

1620-13

FIGURE 14

DCT block and the pixel coordinates for the 1 280 × 720-line system

1620-14

FIGURE 15

DCT block arrangement for the 1 920 × 1 080/60/I system

1620-15

FIGURE 16

DCT block arrangement for the 1 920 × 1 080/50/I system

1620-16
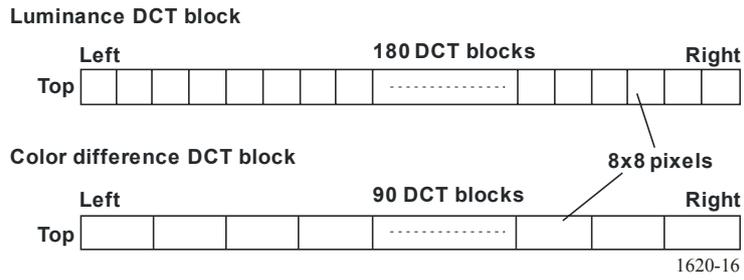
FIGURE 17

DCT block arrangement for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems

1620-17
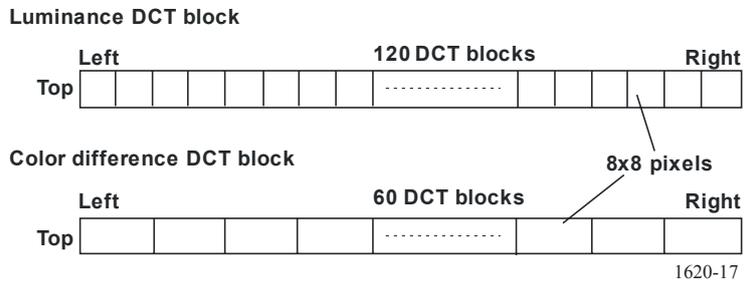
FIGURE 18

Macro block and DCT blocks for the 1 920 × 1 080-line system

1620-18
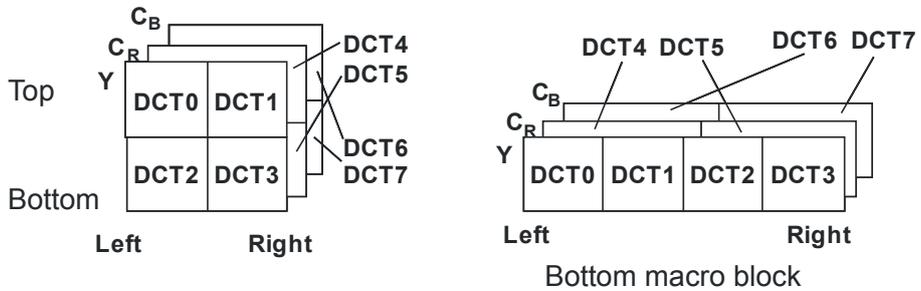
FIGURE 19

Macro block and DCT blocks for the 1 280 × 720-line system

1620-19
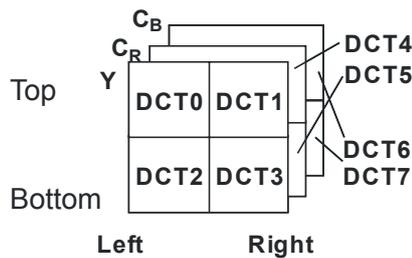
FIGURE 20

Arrangement of macro blocks for the 1 920 × 1 080/60/I system

Step 1: Arranging macro blocks

| 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 macro blocks |

| A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 4 macro blocks |

60 macro blocks

| A8 | A9 | A10 | A11 | A12 | A13 | A14 | A15 | 3 macro blocks |

A16   1 macro block

Bottom macro blocks

Step 2: Rearranging macro blocks

90 macro blocks

60 macro blocks

A0	4 macro blocks
A1	4 macro blocks
A2	4 macro blocks
A3	4 macro blocks
A4	4 macro blocks
A5	4 macro blocks
A6	4 macro blocks
A7	4 macro blocks
A8	3 macro blocks
A9	3 macro blocks
A10	3 macro blocks
A11	3 macro blocks
A12	3 macro blocks
A13	3 macro blocks
A14	3 macro blocks
A15	3 macro blocks
B16	4 macro blocks

10 macro blocks

Rearranging A16 to B16

A16

| 0 | 1 | 2 | 3 | ... | 38 | 39 |

B16

0	1	2	...	8	9
10	11	12	...	18	19
20	21	22	...	28	29
30	31	32	...	38	39
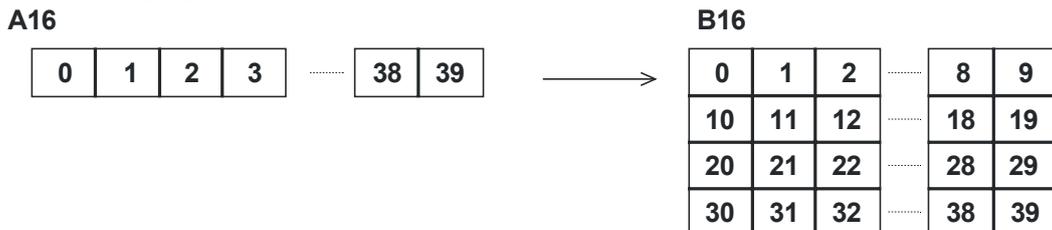
1620-20

FIGURE 21

Arrangement of macro blocks for the 1 920 × 1 080/50/I system

Step 1: Arranging macro blocks
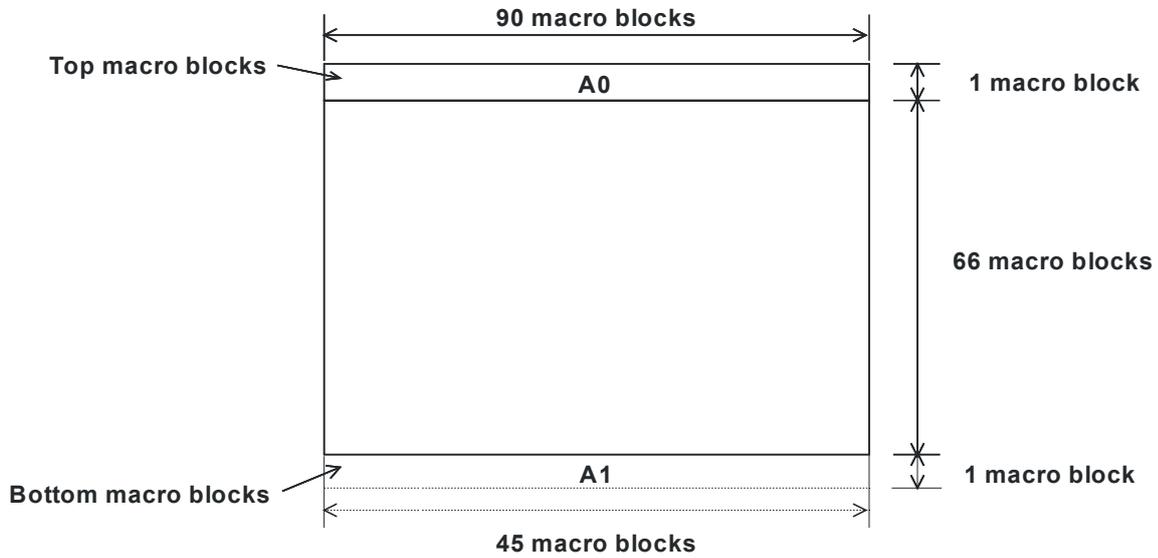
Step 2: Rearranging macro blocks
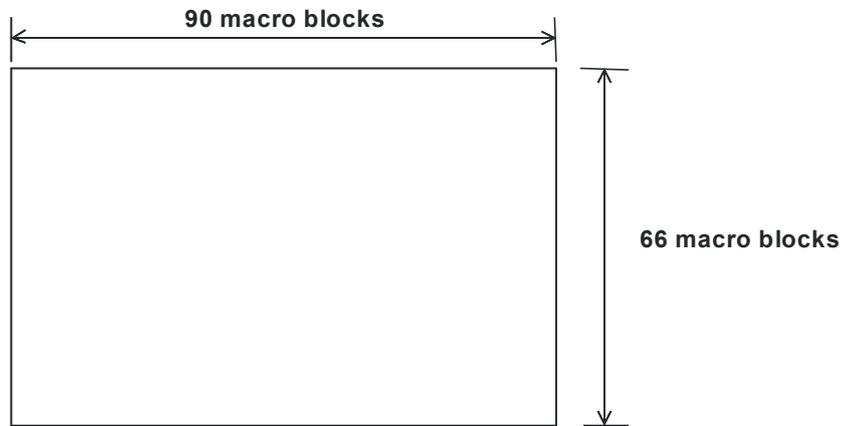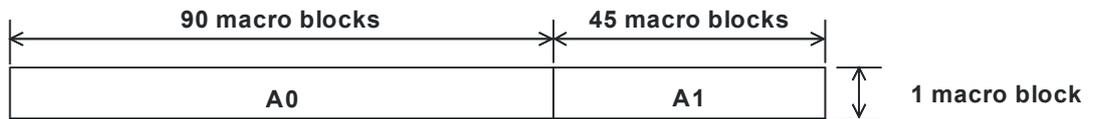
1620-21

FIGURE 22

Arrangement of macro blocks for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems
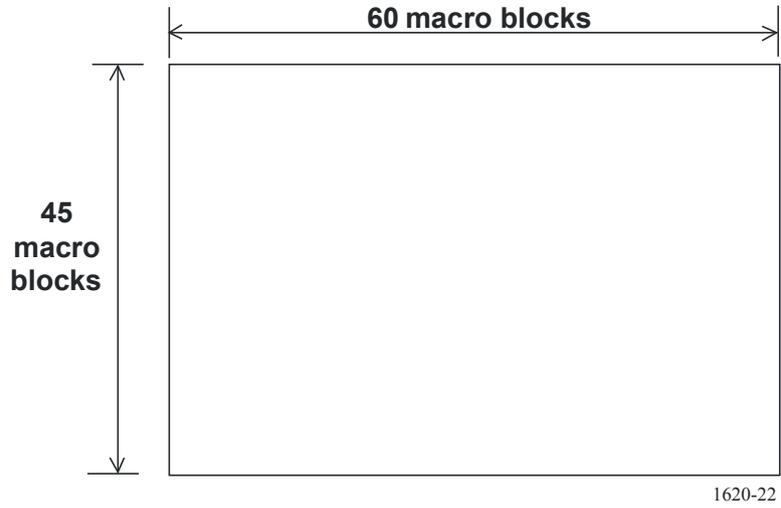
1620-22

FIGURE 23

Divided blocks for the 1 920 × 1 080/60/I system

divided block h=0

divided block h=1

divided block h=2

divided block h=3
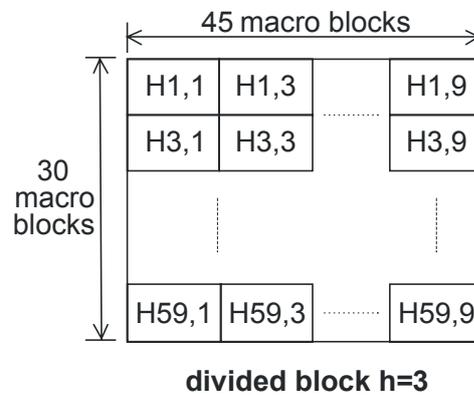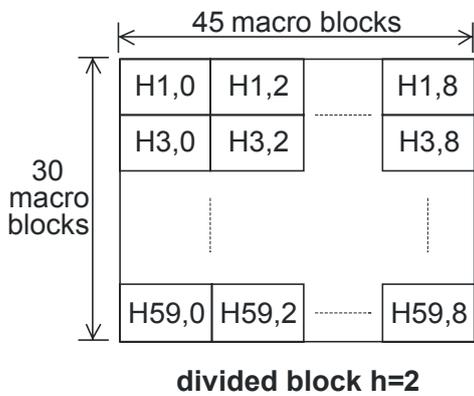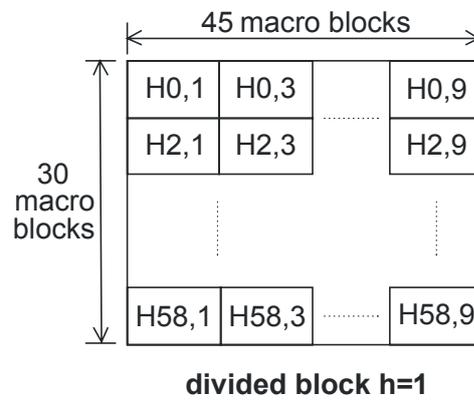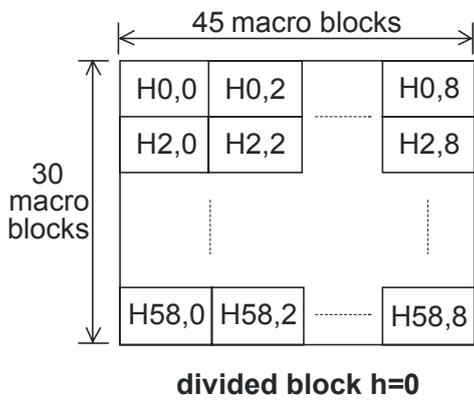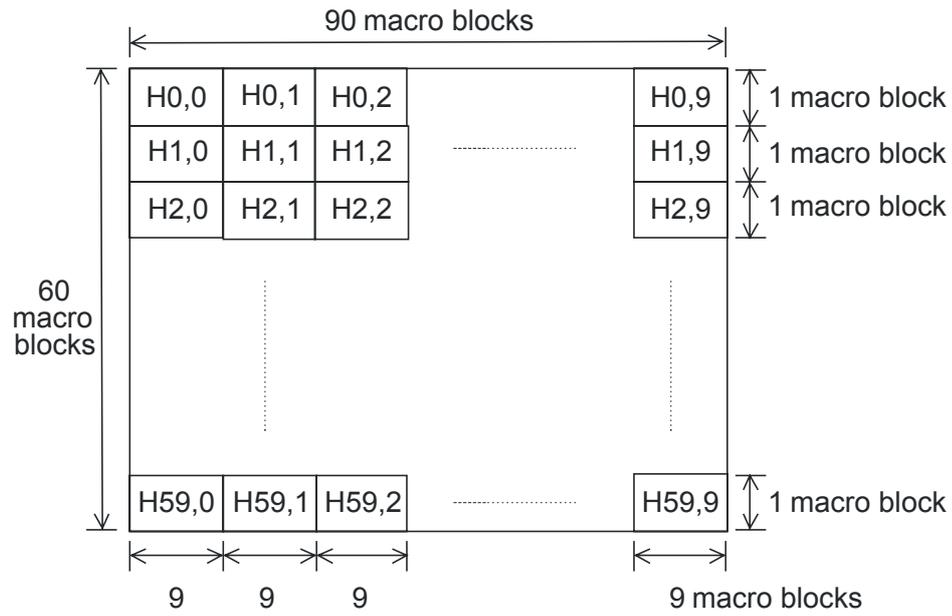
1620-23

FIGURE 24

Divided blocks for the 1 920 × 1 080/50/I system

main unit
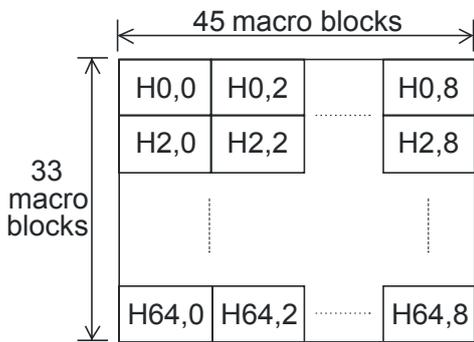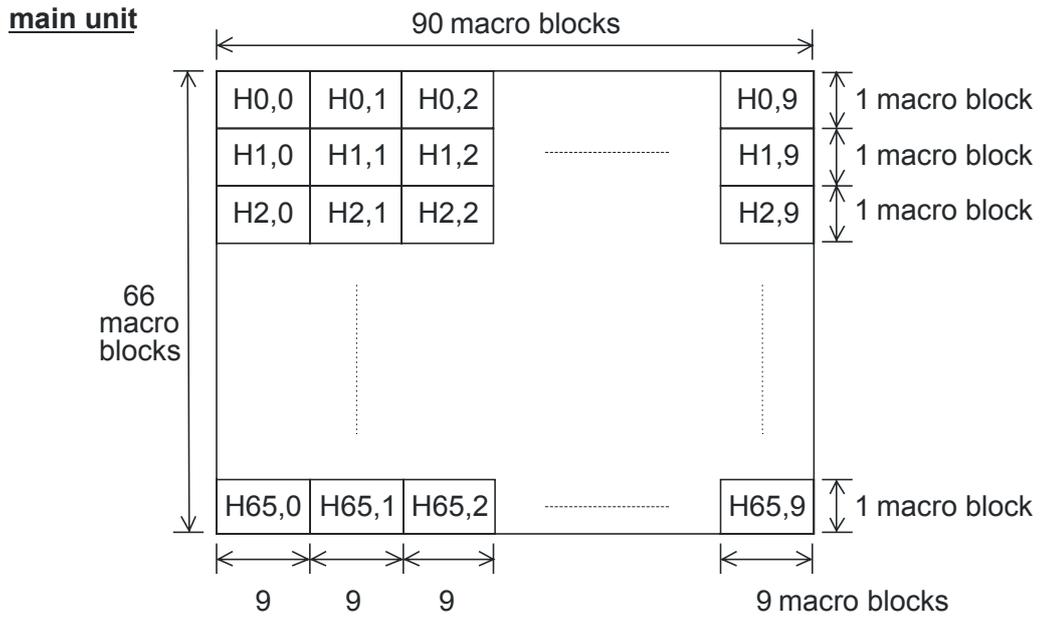
divided block h=0
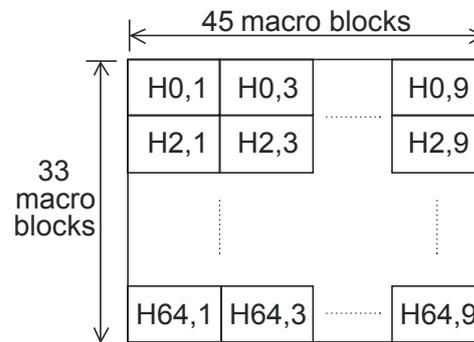
divided block h=1
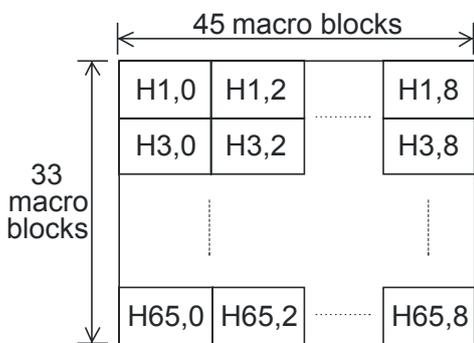
divided block h=2
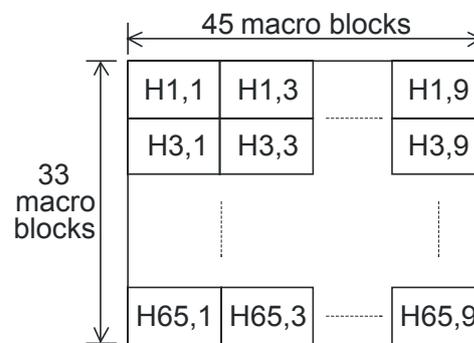
divided block h=3

1620-24

FIGURE 25

Divided blocks for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems
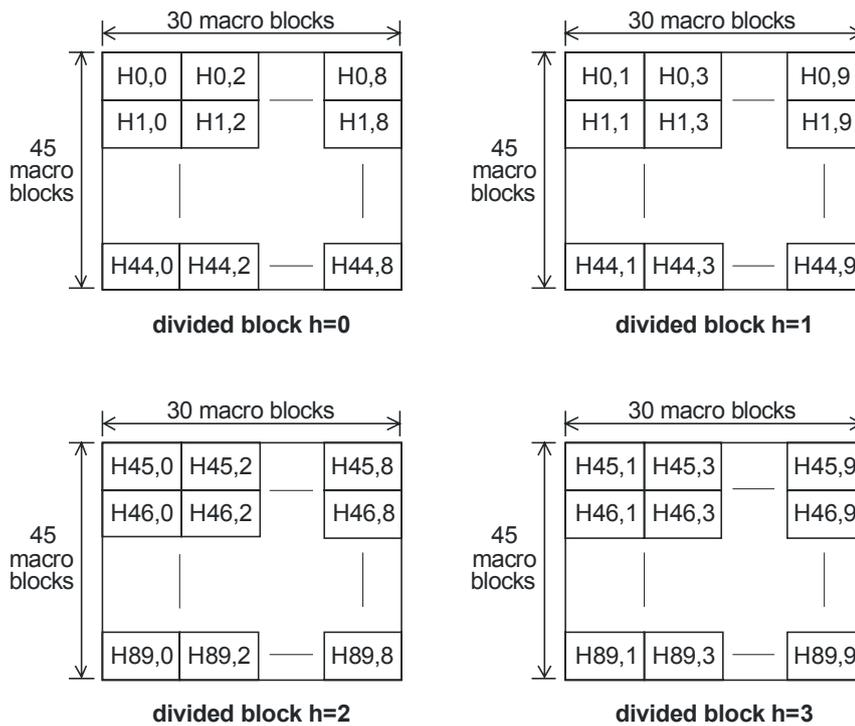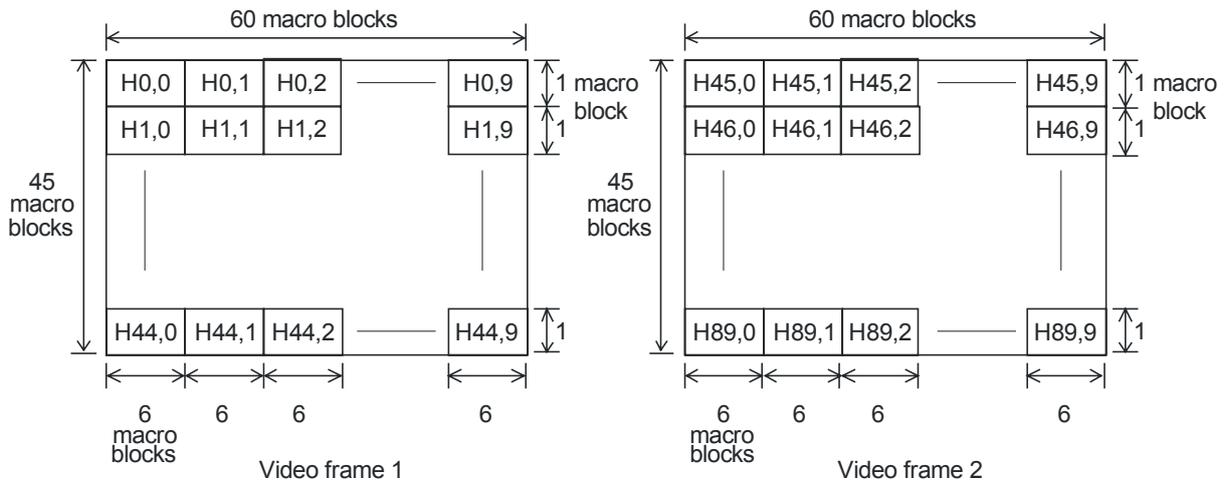
1620-25

4.1.4 Super block

Each super block shall consist of 27 macro blocks.

1 920 × 1 080/60/I system

The arrangement of the super blocks in the divided block shall be as shown in Fig. 26. The pixels in the divided block shall be divided into 50 super blocks.

10 vertical super blocks × 5 horizontal super blocks = 50 super blocks.

1 920 × 1 080/50/I system

The arrangement of the super blocks in the divided block shall be as shown in Fig. 28. The pixels in the divided block shall be divided into 55 super blocks.

11 vertical super blocks × 5 horizontal super blocks = 55 super blocks.

The pixels in the edge unit shall be divided into 5 super blocks.

1 vertical super blocks × 5 horizontal super blocks = 5 super blocks.

1 280 × 720/60/P and 1 280 × 720/50/P systems

The arrangement of the super blocks in the divided block shall be as shown in Fig. 30. The pixels in the divided block shall be divided into 50 super blocks.

10 vertical super blocks × 5 horizontal super blocks = 50 super blocks.

4.1.5 Definition of super block number, macro block number and value of the pixel

Super block number – The super block number is expressed as S h,i,j shown in Figs 26, 28, and 30.

S h,i,j   where   h: the divided block $h = 0, …, 3$

i: the vertical order of the super block $i = 0, …,. 9$ for 60-Hz and 1280 × 720/50/P systems

$i = 0, …, 11$ for 1 920 × 1 080/50/I system

j: the horizontal order of the super block $j = 0, …, 4$

Macro block number – The macro block number is expressed as M h,i,j,k. The symbol k is the macro block order in the super block shown in Fig. 27 for the 1 920 × 1 080/60/I system, Fig. 29 for the 1 920 × 1 080/50/I system, and Fig. 31 for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems. The small rectangle in these figures shows the macro block, and a number in the small rectangle expresses k.

M h,i,j,k   where   h,i, j: the super block number

k: the macro block order in the super block $k = 0, …, 26$

Pixel location – The pixel location is expressed as P h,i,j,k,l(x,y). The pixel is indicated as the suffix of h, i, j, k, l (x, y). The symbol l is the DCT block order in a macro block shown in Figs 18 and 19. The rectangle in the figure shows a DCT block, and a DCT number in the rectangle expresses I. The symbol x and y are the pixel coordinate in the DCT block as described in § 4.1.2.

P h,i,j,k,l(x,y)   where   h,i, j, k: the macro block number

l: the DCT block order in the macro block

(x, y): the pixel coordinate in the DCT block $x = 0, …, 7$ $y = 0, …, 7$.

FIGURE 26

Super blocks and macro blocks in a divided block for the 1 920 × 1 080/60/I system

	Left			j	Right
	0	1	2	3	4
Top 0	Sh,0,0	Sh,0,1	Sh,0,2	Sh,0,3	Sh,0,4
1	Sh,1,0	Sh,1,1	Sh,1,2	Sh,1,3	Sh,1,4
2	Sh,2,0	Sh,2,1	Sh,2,2	Sh,2,3	Sh,2,4
3	Sh,3,0	Sh,3,1	Sh,3,2	Sh,3,3	Sh,3,4
4	Sh,4,0	Sh,4,1	Sh,4,2	Sh,4,3	Sh,4,4
5	Sh,5,0	Sh,5,1	Sh,5,2	Sh,5,3	Sh,5,4
6	Sh,6,0	Sh,6,1	Sh,6,2	Sh,6,3	Sh,6,4
7	Sh,7,0	Sh,7,1	Sh,7,2	Sh,7,3	Sh,7,4
8	Sh,8,0	Sh,8,1	Sh,8,2	Sh,8,3	Sh,8,4
9	Sh,9,0	Sh,9,1	Sh,9,2	Sh,9,3	Sh,9,4

Bottom

3 macro blocks

Super block i=9 j=1
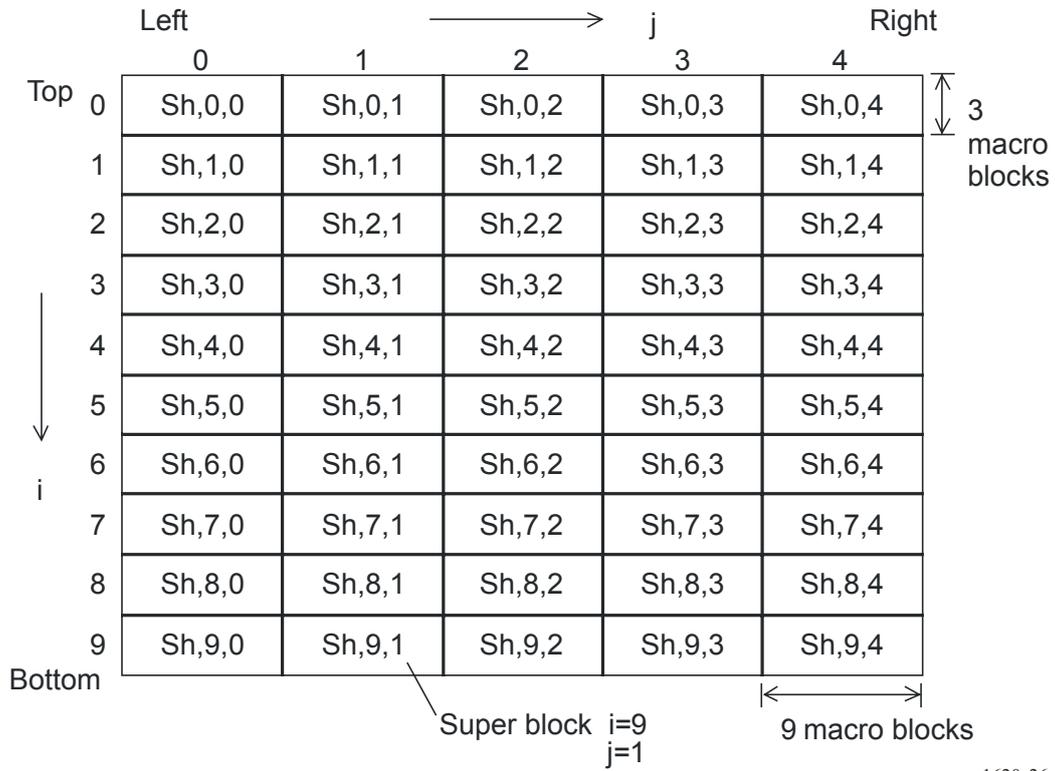
9 macro blocks

1620-26

FIGURE 27

Macro block order in a super block for the 1 920 × 1 080/60/I system

Super block Sh,i,j (h=0,...,3, i=0,...,9, j=0,...,4)

0	1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16	17
18	19	20	21	22	23	24	25	26

k

1620-27

FIGURE 28

Super blocks and macro blocks for the 1 920 × 1 080/50/I system

divided block

	Left 0	1	2	3	Right 4	
Top 0	Sh,0,0	Sh,0,1	Sh,0,2	Sh,0,3	Sh,0,4	3 macro blocks
1	Sh,1,0	Sh,1,1	Sh,1,2	Sh,1,3	Sh,1,4	
2	Sh,2,0	Sh,2,1	Sh,2,2	Sh,2,3	Sh,2,4	
3	Sh,3,0	Sh,3,1	Sh,3,2	Sh,3,3	Sh,3,4	
4	Sh,4,0	Sh,4,1	Sh,4,2	Sh,4,3	Sh,4,4	
5	Sh,5,0	Sh,5,1	Sh,5,2	Sh,5,3	Sh,5,4	
6	Sh,6,0	Sh,6,1	Sh,6,2	Sh,6,3	Sh,6,4	
7	Sh,7,0	Sh,7,1	Sh,7,2	Sh,7,3	Sh,7,4	
8	Sh,8,0	Sh,8,1	Sh,8,2	Sh,8,3	Sh,8,4	
9	Sh,9,0	Sh,9,1	Sh,9,2	Sh,9,3	Sh,9,4	
10 Bottom	Sh,10,0	Sh,10,1	Sh,10,2	Sh,10,3	Sh,10,4	

Super block i=10 j=1
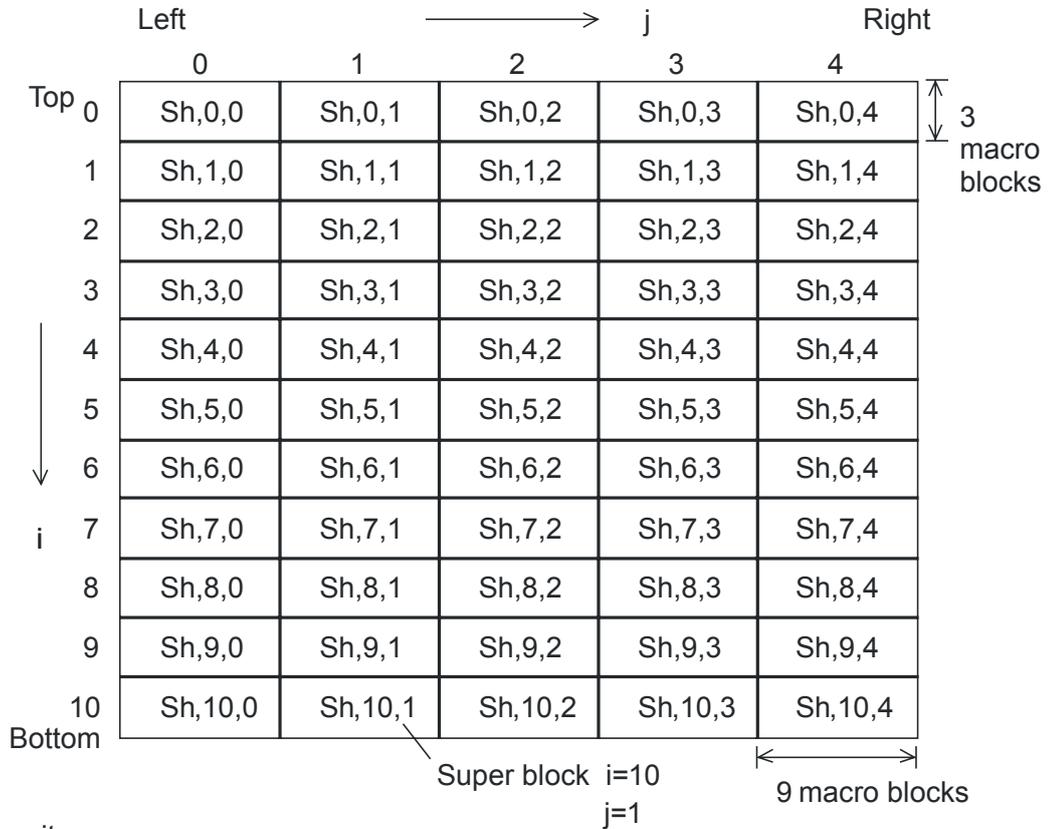
9 macro blocks

edge unit

S 0,11,0	S 0,11,1	S 0,11,2	S 0,11,3	S 0,11,4

1620-28

FIGURE 29

Macro block order in a super block for the 1 920 × 1 080/50/I system

Super block Sh,i,j (h=0,...,3, i=0,...,10, j=0,...,4)

0	1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16	17
18	19	20	21	22	23	24	25	26

k

Super block S 0,11,j (j=0,...,4)

0	1	2	....	26

1620-29

FIGURE 30

**Super blocks and macro blocks in a divided block
for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems**
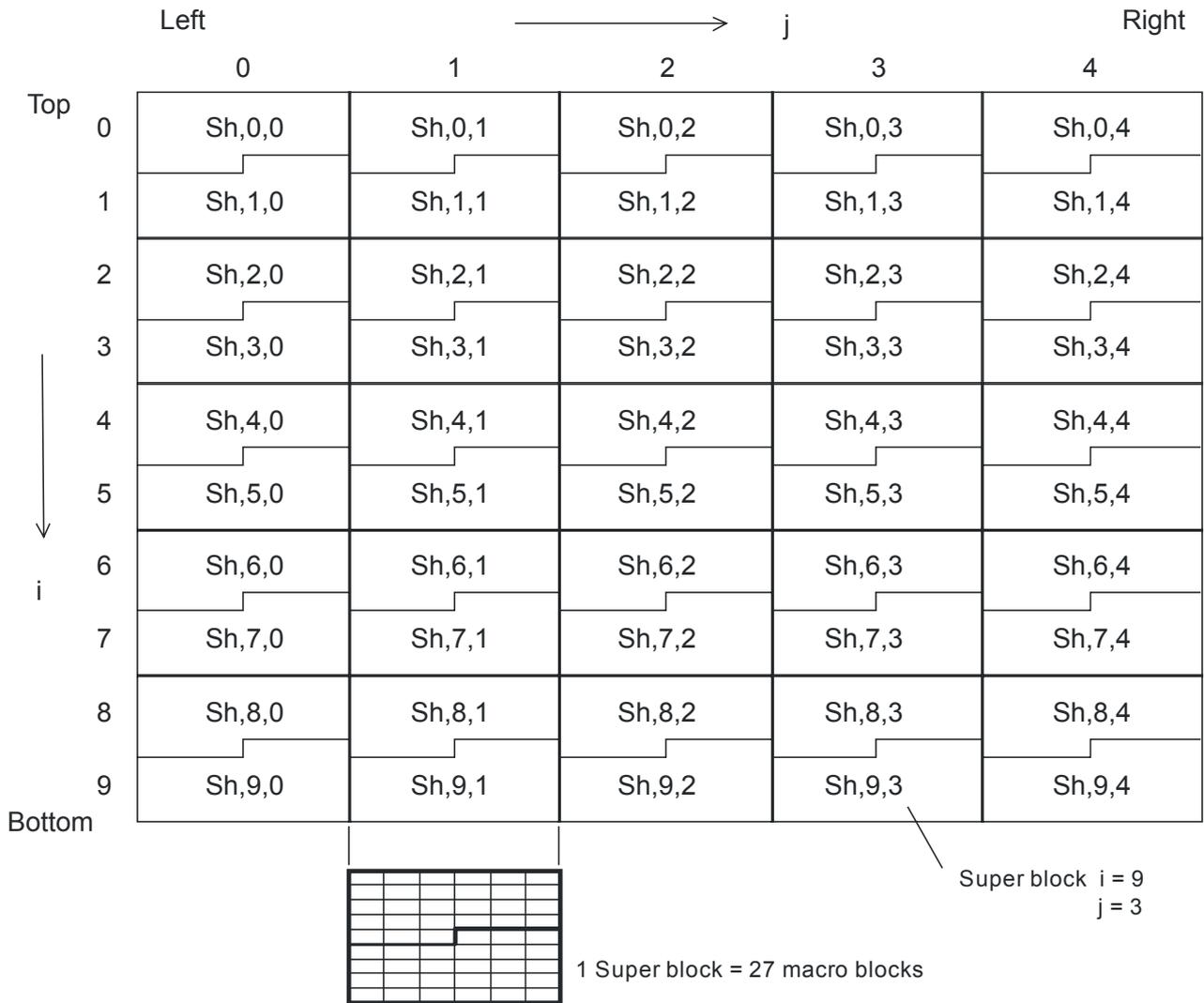
1620-30

FIGURE 31

Macro block order in a super block for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems

Super block Sh,i,j (h=0,...,3, i=0,...,9, j=0,...,4)

1620-31

4.1.6   Definition of video segment and compressed macro block

The video segment shall consist of five macro blocks which are assembled from various areas within the video frame.

60-Hz system

M h,a,p,k   where a = (i + 2) mod 10, p = 2

M h,b,q,k   where b = (i + 6) mod 10, q = 1

M h,c,r,k   where c = (i + 8) mod 10, r = 3

M h,d,s,k   where d = (i + 0) mod 10, s = 0

M h,e,t,k   where e = (i + 4) mod 10, t = 4

where   h: the divided block   h = 0, …, 3

          i: the vertical order of the super block   i = 0, …, 9

          k: the macro block order in the super block   k = 0, …, 26

50-Hz system

divided block

M h,a,p,k   where a = (i + 2) mod 11, p = 2

M h,b,q,k   where b = (i + 6) mod 11, q = 1

M h,c,r,k   where c = (i + 8) mod 11, r = 3

M h,d,s,k   where d = (i + 0) mod 11, s = 0

M h,e,t,k   where e = (i + 4) mod 11, t = 4

where   h: the divided block   h = 0, …, 3

          i: the vertical order of the super block   i = 0, …, 10

          k: the macro block order in the super block   k = 0, …, 26

edge unit

M h,a,p,k   where h = 0, a = 11, p = 0

M h,b,q,k   where h = 0, b = 11, q = 1

M h,c,r,k   where h = 0, c = 11, r = 2

M h,d,s,k   where h = 0, d = 11, s = 3

M h,e,t,k   where h = 0, e = 11, t = 4

where   k: the macro block order in the super block   k = 0, …, 26

Each video segment before the bit rate reduction is expressed as V h,i,k which consists of M h,a,p,k; M h,b,q,k; M h,c,r,k; M h,d,s,k; and M h,e,t,k.

The bit-rate reduction process shall be operated sequentially from M h,a,p,k to M h,e,t,k. The data in the video segment shall be compressed and transformed to a 385-byte data stream. A set of compressed video data consists of five compressed macro blocks. Each compressed macro block shall consist of 77 bytes and is expressed as CM. Each video segment after the bit-rate reduction is expressed as CV h,i,k which consists of CM h,a,p,k; CM h,b,q,k; CM h,c,r,k; CM h,d,s,k; and CM h,e,t,k as shown below:

CM h,a,p,k:

This block includes all parts or most parts of the compressed data from macro block M h,a,p,k and may include the compressed data of macro block M h,b,q,k; or M h,c,r,k; or M h,d,s,k; or M h,e,t,k.

CM h,b,q,k:

This block includes all parts or most parts of the compressed data from macro block M h,b,q,k and may include the compressed data of macro block M h,a,p,k; or M h,c,r,k; or M h,d,s,k; or M h,e,t,k.

CM h,c,r,k:

This block includes all parts or most parts of the compressed data from macro block M h,c,r,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,d,s,k; or M h,e,t,k.

CM h,d,s,k:

This block includes all parts or most parts of the compressed data from macro block M h,d,s,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,c,r,k; or M h,e,t,k.

CM h,e,t,k:

This block includes all parts or most parts of the compressed data from macro block M h,e,t,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,c,r,k; or M h,d,s,k.

4.2   DCT processing

Four rows of eight horizontal pixels from each field of a video frame form the DCT block in the 1 920 × 1 080-line system. Eight rows of eight horizontal pixels from a video frame form the DCT block in the 1 280 × 720-line system.

The DCT transformation from 64 pixels in a DCT block whose numbers are h, i, j, k, l (x, y) to 64 coefficients whose numbers are h, i, j, k, l (u, v) is described as follows:

P h,i,j,k,l(x,y) is the value of the pixel and C h,i,j,k,l(u,v) is the value of the coefficient.

For u = 0 and v = 0, the coefficient is called DC coefficient.

All other coefficients are called AC coefficients.

4.2.1   DCT mode

For the 1 920 × 1 080-line system, one of two DCT modes is selected for purpose to improve picture quality after bit rate reduction. These modes are defined as the 8-8-frame-DCT mode and the 8-8-field-DCT mode. The 8-8-frame-DCT mode should be selected when the difference between two fields in a video frame is small. The 8-8-field-DCT mode should be selected when the difference between two fields in a video frame is large.

For the DCT blocks in the bottom macro block in the 1 920 × 1 080/60/I system, it is recommended to select the 8-8-frame–DCT mode.

For the 1 280 × 720-line system, the 8-8-frame-DCT mode should be selected.

The same DCT mode shall be applied to all DCT blocks in a macro block.

As shown in Fig. 32, if the 8-8-field-DCT mode is selected, pixels in the two vertical adjacent DCT blocks shall be rearranged to form the re-arranged DCT blocks that contain pixels from the same field.

The following DCT paragraph shows the algorithm that is applied to both DCT modes, the 8-8-frame-DCT and the 8-8-field-DCT modes.

DCT:

$$C_{h,i,j,k,l}(u,v) = C(v) \, C(u) \sum_{y=0}^{7} \sum_{x=0}^{7} (P_{h,i,j,k,l}(x,y) \, \cos(\pi v(2y + 1) / 16) \, \cos(\pi u(2x + 1) / 16))$$

Inverse DCT:

$$P_{h,i,j,k,l}(x,y) = \sum_{v=0}^{7} \sum_{u=0}^{7} (C(v) \, C(u) \, C_{h,i,j,k,l}(u,v) \, \cos(\pi v(2y + 1) / 16) \, \cos(\pi u(2x + 1) / 16))$$

where:

$$C(u) = 0.5 / \sqrt{2} \quad \text{for } u = 0$$
$$C(u) = 0.5 \quad \text{for } u = 1 \text{ to } 7$$
$$C(v) = 0.5 / \sqrt{2} \quad \text{for } v = 0$$
$$C(v) = 0.5 \quad \text{for } v = 1 \text{ to } 7.$$

The values of the DCT coefficients $C_{h,i,j,k,l}(u,v)$ are represented with 16 bits. Before weighting, therefore, the DCT coefficients shall be scaled depending on the sample resolution of the DCT input.

FIGURE 32

Rearrangement of pixels in the 8-8-field-DCT mode
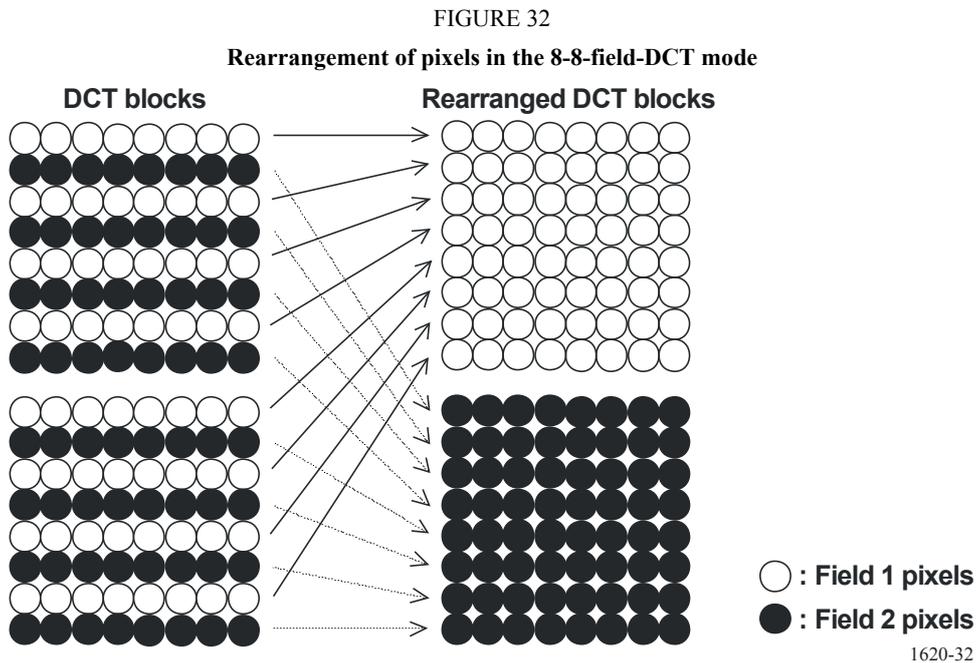
4.2.2 Weighting

The DCT coefficients $C_{h,i,j,k,l}(u,v)$ shall be weighted by quantizer matrix. The different quantizer matrices shall be set for luminance signals and colour difference signals as shown in Fig. 33 for the 1 920 × 1 080/60/I system, Fig. 34 for the 1 920 × 1 080/50/I system and Fig. 35 for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems.

4.2.3 Output order

Figure 36 shows the output order of the weighted coefficients.

FIGURE 33

Quantizer matrix for the 1 920 × 1 080/60/I system

Luminance — Horizontal

	0	1	2	3	4	5	6	7
0	128	16	17	18	18	19	42	44
1	16	17	18	18	19	38	43	45
2	17	18	19	19	40	41	45	48
3	18	18	19	40	41	42	46	49
4	18	19	40	41	42	43	48	101
5	19	38	41	42	43	44	98	104
6	42	43	45	46	48	98	109	116
7	44	45	48	49	101	104	116	123

Vertical (arrow downward)

Color difference — Horizontal

	0	1	2	3	4	5	6	7
0	128	16	17	25	26	26	42	44
1	16	17	25	25	26	38	43	91
2	17	25	26	27	40	41	91	96
3	25	25	27	40	41	84	93	197
4	26	26	40	41	84	86	191	203
5	26	38	41	84	86	177	197	209
6	42	43	91	93	191	197	219	232
7	44	91	96	197	203	209	232	246

Vertical (arrow downward)

1620-33

FIGURE 34

Quantizer matrix for the 1 920 × 1 080/50/I system

Luminance — Horizontal

	0	1	2	3	4	5	6	7
0	128	16	17	18	18	19	42	44
1	16	17	18	18	19	38	43	45
2	17	18	19	19	40	41	45	48
3	18	18	19	40	41	42	46	49
4	18	19	40	41	42	43	48	101
5	19	38	41	42	43	44	98	104
6	42	43	45	46	48	98	109	116
7	44	45	48	49	101	104	116	123

Vertical (arrow downward)

Color difference — Horizontal

	0	1	2	3	4	5	6	7
0	128	16	17	25	26	26	42	44
1	16	17	25	25	26	38	43	91
2	17	25	26	27	40	41	91	96
3	25	25	27	40	41	84	93	197
4	26	26	40	41	84	86	191	203
5	26	38	41	84	86	177	197	209
6	42	43	91	93	191	197	219	232
7	44	91	96	197	203	209	232	246

Vertical (arrow downward)

1620-34

FIGURE 35

Quantizer matrix for the 1 280 × 720/60/P and the 1 280 × 720/50/P systems

Luminance — Horizontal

	0	1	2	3	4	5	6	7
0	128	16	17	18	18	19	42	44
1	16	17	18	18	19	38	43	68
2	17	18	19	19	40	41	68	96
3	18	18	19	40	41	63	92	98
4	18	19	40	41	63	86	96	202
5	19	38	41	63	86	88	196	208
6	42	43	68	92	96	196	218	232
7	44	68	96	98	202	208	232	246

Vertical (arrow downward)

Color difference — Horizontal

	0	1	2	3	4	5	6	7
0	128	24	26	36	36	38	84	88
1	24	26	36	36	38	76	86	182
2	26	36	38	38	80	82	182	192
3	36	36	38	80	82	168	186	394
4	36	38	80	82	168	192	382	406
5	38	76	82	168	172	354	394	418
6	84	86	182	186	382	394	438	464
7	88	182	192	394	406	418	464	492

Vertical (arrow downward)

1620-35

FIGURE 36

Output order of weighted DCT coefficients

1620-36

4.3 Quantization

4.3.1 Introduction

The weighted DCT coefficients shall be divided by quantization steps in order to limit the amount of data in one video segment to five compressed macro blocks and limit the bit length of the AC coefficients within 9 bits.

4.3.2 Bit assignment for quantization

The weighted DCT coefficients shall be represented as follows:

DC coefficient value (9 bits): b8 b7 b6 b5 b4 b3 b2 b1 b0

twos complement (−255 to 255)

AC coefficient value (12 bits): s b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0

1 sign bit + 11 bits of absolute value (−2 047 to 2 047).

4.3.3 Quantization step

The quantization step (Q-step) is selected in order to limit the amount of data in each five compressed macro blocks which are generated from a single video segment. Q-step shall be decided by the quantization number (QNO) and class number as specified in Table 26. The QNO shall be applied to every macro block. The class number shall be applied to every DCT block.

Data reduction consists of two procedures. First, the AC coefficient is divided by the Q-step. If the bit length of the quantized AC coefficient obtained is more than 9, then the second procedure is performed. In the second procedure, the AC coefficient is divided again by larger Q-step according to increasing class numbers in order to make the bit length of the quantized AC coefficient 9 or less.

TABLE 26

Quantization step

		Class number			
		0	1	2	3
Quantization number (QNO)	1	1	2	4	8
	2	2	4	8	
	3	3	6	12	
	4	4	8		
	5	5	10		
	6	6	12		
	7	7	14		
	8	8			
	9	16	32	64	
	10	18	36	72	
	11	20	40	80	
	12	22	44	88	
	13	24	48	96	
	14	28	56	112	
	15	52	104		

4.4   Variable length coding (VLC)

Variable length coding is an operation for transforming from quantized AC coefficients to variable length codes. One or more successive AC coefficients within a DCT block shall be coded into one variable length code according to the order as shown in Fig. 36. Run length and amplitude are defined as follows:

Run length: The number of successive AC coefficients quantized to 0

(run = 0, …, 61)

Amplitude: Absolute value just after successive AC coefficients quantized to 0

(amp = 0, …, 255)

(run, amp): The pair of run length and amplitude.

Table 27 shows the length of code words corresponding to (run, amp). In Table 27, sign bit is not included in the length of code words. When the amplitude is not zero, the code length is incremented by one to express the sign bit of the amplitude. For empty cells in Table 27, the code word of the (run, amp) is expressed by a combination of the (run – 1, 0) and the (0, amp).

Code words for (run.amp) shall be assigned as shown in Table 28. The leftmost bit of code words is MSB and the rightmost bit of code words is LSB in Table 28. The MSB of a subsequent code word is next to the LSB of the code word just before. Sign bit "s" shall be set as follows.

When the quantized AC coefficient is greater than zero, s = 0.

When the quantized AC coefficient is less than zero, s = 1.

When the values of all of the remaining quantized coefficients are zero within a DCT block, the coding process is ended by adding the EOB (end of block) code word of 0110b immediately after the last code word.

TABLE 27

Length of codewords

Run length	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	------	255
																									Amplitude	
0	11	2	3	4	4	5	5	6	6	7	7	7	8	8	8	8	8	8	9	9	9	9	9	15	------	15
1	11	4	5	7	7	8	8	8	9	10	10	10	11	11	11	12	12	12								
2	12	5	7	8	9	9	10	12	12	12	12	12														
3	12	6	8	9	10	10	11	12																		
4	12	6	8	9	11	12																				
5	12	7	9	10																						
6	13	7	9	11																						
7	13	8	12	12																						
8	13	8	12	12																						
9	13	8	12																							
10	13	8	12																							
11	13	9																								
12	13	9																								
13	13	9																								
14	13	9																								
15	13																									
⋮	⋮																									
61	13																									

NOTES

1 Sign bit is not included.

2 The length of EOB = 4.

TABLE 28

Codewords of variable length coding

(Run, amp)		Code	Length	(Run, amp)		Code	Length	(Run, amp)		Code	Length
0	1	00s	2+1	11	1	111100000s	9+1	7	2	111110110000s	12+1
0	2	010s	3+1	12	1	111100001s		8	2	111110110001s	
EOB		0110	4	13	1	111100010s		9	2	111110110010s	
1	1	0111s	4+1	14	1	111100011s		10	2	111110110011s	
0	3	1000s		5	2	111100100s		7	3	111110110100s	
0	4	1001s		6	2	111100101s		8	3	111110110101s	
2	1	10100s	5+1	3	3	111100110s		4	5	111110110110s	
1	2	10101s		4	3	111100111s		3	7	111110110111s	
0	5	10110s		2	4	111101000s		2	7	111110111000s	
0	6	10111s		2	5	111101001s		2	8	111110111001s	
3	1	110000s	6+1	1	8	111101010s		2	9	111110111010s	
4	1	110001s		0	18	111101011s		2	10	111110111011s	
0	7	110010s		0	19	111101100s		2	11	111110111100s	
0	8	110011s		0	20	111101101s		1	15	111110111101s	
5	1	1101000s	7+1	0	21	111101110s		1	16	111110111110s	
6	1	1101001s		0	22	111101111s		1	17	111110111111s	
2	2	1101010s		5	3	1111100000s	10+1	6	0	1111110000110	13
1	3	1101011s		3	4	1111100001s		7	0	1111110000111	13
1	4	1101100s		3	5	1111100010s		R	0	1111110 / Binary notation of R, R = 6 to 61	13
0	9	1101101s		2	6	1111100011s		61	0	1111110111101	13
0	10	1101110s		1	9	1111100100s					
0	11	1101111s		1	10	1111100101s					

TABLE 28 (*end*)

(Run, amp)		Code	Length	(Run, amp)		Code	Length	(Run, amp)		Code	Length
7	1	11100000s	8+1	1	11	1111100110s	11	0	23	111111100010111s	15+1
8	1	11100001s		0	0	11111001110		0	24	111111100011000s	
9	1	11100010s		1	0	11111001111					
10	1	11100011s		6	3	11111010000s	11+1	0	A	111111 1 — Binary notation of A, A = 23 to 255 — s	15+1
3	2	11100100s		4	4	11111010001s					
4	2	11100101s		3	6	11111010010s		0	255	111111111111111s	
2	3	11100110s		1	12	11111010011s					
1	5	11100111s		1	13	11111010100s					
1	6	11101000s		1	14	11111010101s					
1	7	11101001s		2	0	111110101100	12				
0	12	11101010s		3	0	111110101101					
0	13	11101011s		4	0	111110101110					
0	14	11101100s		5	0	111110101111					
0	15	11101101s									
0	16	11101110s									
0	17	11101111s									

4.5   Arrangement of a compressed macro block

The compressed video segment shall consist of five compressed macro blocks. Each compressed macro block has 77 bytes of data. The arrangement of the compressed macro block shall be as shown in Fig. 37.

STA (status of the compressed macro block).

STA expresses the error and concealment information of the compressed macro block and shall consist of four bits: s3, s2, s1, s0. Table 29 shows the definitions of STA.

QNO (quantization number) – QNO is the quantization number applied to the macro block. Code words of the QNO shall be as shown in Table 30.

DC

DCl (where l is the DCT block order in the macro block, l = 0, …, 7) shall consist of a DC coefficient, the DCT mode, and the class number of the DCT block.

```
        MSB                              LSB
     DCl :  b8  b7  b6  b5  b4  b3  b2  b1  b0  mo  c1  c0
where
     b8 to b0:  DC coefficient value
      mo : DCT mode
         for l = 0   0 = 8-8-frame-DCT mode
                     1 = 8-8-field-DCT mode
        for l = 1 to 7 reserved bit for future use
               Default value shall be set to 1
     c1 c0 : class number
```

AC

AC is a generic term for variable length coded AC coefficients within the video segment V h,i,k. The areas of Y_0, Y_1, Y_2, Y_3, C_{R0}, C_{R1}, C_{B0}, and C_{B1} are defined as compressed-data areas, each of Y_0, Y_1, Y_2, Y_3, C_{R0}, and C_{R1} shall consist of 80 bits and each C_{B0} and C_{B1} shall consist of 64 bits as shown in Fig. 37. DCI and variable length code for AC coefficients in the DCT block whose DCT block number is h,i,j,k,l shall be assigned from the beginning of the compressed-data area in the compressed macro block CM h,i,j,k. In Fig. 37, the variable length code word is located starting

from MSB which is shown in the upper left side, and the LSB shown in the lower right side. Therefore, AC data are distributed from the upper left corner to the lower right corner.

FIGURE 37

Arrangement of a compressed macro block

Byte position number

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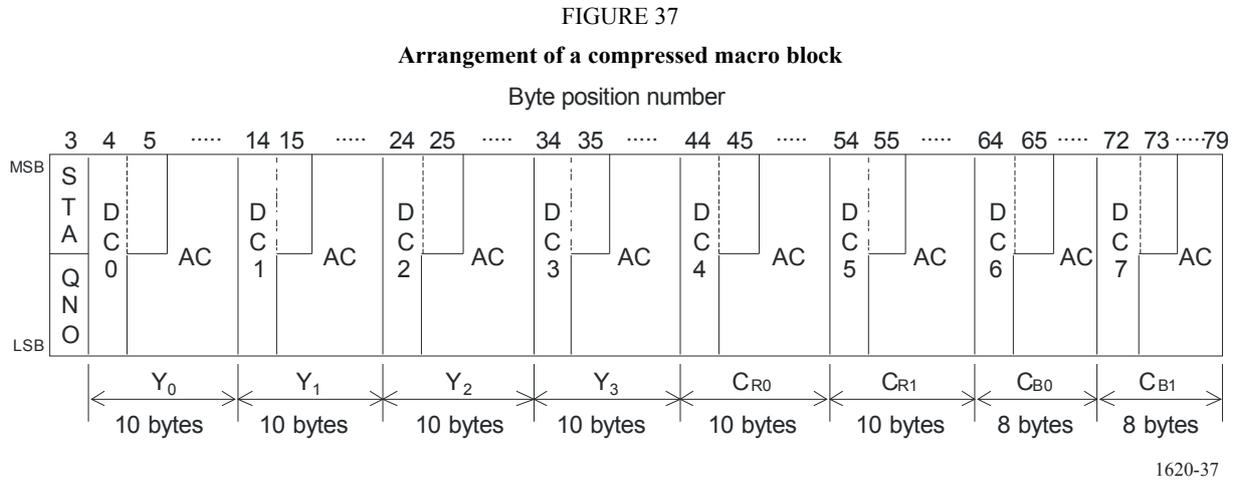
TABLE 29

Definition of STA

STA bit				Information of the compressed macro block		
s3	s2	s1	s0	Error	Error concealment	Continuity
0	0	0	0		Not proceeded	———
0	0	1	0	No error	Type A	Type a
0	1	0	0		Type B	
0	1	1	0		Type C	
0	1	1	1	Error exists	———	———
1	0	1	0	No error	Type A	Type b
1	1	0	0		Type B	
1	1	1	0		Type C	
1	1	1	1	Error exists	———	———
other				reserved		

where

Type A: Replaced with a compressed macro block of the same compressed macro block number in the frame immediately previous.

Type B: Replaced with a compressed macro block of the same compressed macro block number in the next immediate frame.

Type C: This compressed macro block is concealed, but the concealment method is not specified.

Type a: The continuity of data processing sequence with other compressed macro block whose s0 = 0 and s3 = 0 in the same video segment is guaranteed.

Type b: The continuity of data processing sequence with other compressed macro block is not guaranteed.

NOTES

1 For STA = 0111b, the error code is inserted in the compressed macro block. This is an option.

2 For STA = 1111b, the error position is unidentified.

TABLE 30

Codewords of the QNO

Q number bit				QNO
q3	q2	q1	q0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

4.6   Arrangement of a video segment

In this section, the distribution method of quantized AC coefficients is described. The video segment CV h,i,k after bit-rate reduction shall be arranged as shown in Fig. 38. The column shows the compressed macro block. Symbol F h,i,j,k,l expresses a compressed data area for the DCT block whose DCT block number is h, i, j, k, l. Bit sequence, defined as B h,i,j,k,l, shall consist of the following concatenated data: DC coefficient, DCT mode information, class number, and AC coefficient code words for DCT blocks numbered h,i,j,k,l. Code words for AC coefficients of B h,i,j,k,l shall be concatenated according to the order as shown in Fig. 36 and the last code word shall be EOB. The MSB of the subsequent code word shall be next to the LSB of the code word just before it.

The algorithm for the arrangement of the video segment shall be composed of the three passes below:

Pass 1: The distribution of B h,i,j,k,l to the compressed-data area.

Pass 2: The distribution of the overflow B h,i,j,k,l which remains after the pass 1 operation in the same compressed macro block.

Pass 3: The distribution of the overflow B h,i,j,k,l which remains after the pass 2 operation in the same video segment.

Arrangement algorithm of a video segment:

```
for(h = 0;  h < 4;  h ++) {
   if (60 Hz system) n = 10;
   else if (h = 0) n = 12;
   else n = 11;
    for (i = 0;  i < n;  i ++) {
       if (i < 11) {
           a = (i + 2) mod n;
           b = (i + 6) mod n;
           c = (i + 8) mod n;
           d = (i + 0) mod n;
```

```
            e = (i + 4) mod n;
            p = 2; q = 1; r = 3; s = 0; t = 4;
        }
        else {
            a = b = c = d = e = 11;
            p = 0; q = 1; r = 2; s = 3; t = 4;
        }
        for (k = 0;  k < 27; k ++) {
            x = a; y = p;
            VR = 0;
             /* VR is the bit sequence for the data                    */
             /*   which are not distributed to video segment CV h,i,k by pass 2. */
    /* pass 1 */
            for (j = 0;  j < 5; j ++) {
                MRy = 0;
                /* MRy is the bit sequence for the data                    */
                /* which are not distributed to macro block M h,x,y,k by pass 1. */
                for (l = 0;  l < 8; l ++) {
                 remain = distribute (B h,x,y,k,l,  F h,x,y,k,l);
                 MRy = connect (MRy,  remain);
                }
                 if (y == p)  {y = q;  x = b;}
                else if (y == q)  {y = r;  x = c;}
                else if (y == r)  {y = s;  x = d;}
                else if (y == s)  {y = t;  x = e;}
                else if (y == t)  {y = p;  x = a;}
            }
    /* pass 2 */
            for (j = 0;  j < 5; j ++) {
                for (l = 0;  l < 8; l ++) {
                 MRy = distribute (MRy,  F h,x,y,k,l);
                }
                VR = connect (VR,  MRy);
                 if (y == p)  {y = q;  x = b;}
                else if (y == q)  {y = r;  x = c;}
                else if (y == r)  {y = s;  x = d;}
                else if (y == s)  {y = t;  x = e;}
                else if (y == t)  {y = p;  x = a;}
            }
    /* pass 3 */
            for (j = 0;  j < 5; j ++) {
                for (l = 0;  l < 8; l ++) {
                    VR = distribute (VR,  F h,x,y,k,l);
                }
                 if (y == p)  {y = q;  x = b;}
                else if (y == q)  {y = r;  x = c;}
                else if (y == r)  {y = s;  x = d;}
                else if (y == s)  {y = t;  x = e;}
                else if (y == t)  {y = p;  x = a;}
            }
        }
    }
}

where
    distribute (data 0, area 0) {        /* Distribute data 0 from MSB into empty area of area 0. */
                                         /* The area 0 is filled starting from the MSB.          */
        remain = (remaining_data);  /* Remaining_data are the data which are not distributed. */
        return (remain);
    }
    connect (data 1, data 2 ) {        /* Connect the MSB of data 2 with the LSB of data 1.   */
        data 3 = (connecting_data); /*  Connecting_data are the data which are connected.  */
```

```
                        /*  data 2 with data 1.                              */
        return (data3);
    }
```

The remaining data which can not be distributed within the unused space of the macro block will be ignored. Therefore, when error concealment is performed for a compressed macro block, some data distributed by pass 3 may not be reproduced.

Video error code processing

If errors are detected in a compressed macro block which is reproduced and processed with error correction, the compressed-data area containing these errors should be replaced with the video error code. This process replaces the first two bytes of data of the compressed-data area with the code as follows:

    MSB   LSB

    1000000000000110b

The first 9 bits are DC error code, the next 3 bits are the information of DCT mode and class number and the last 4 bits are the EOB as shown in Fig. 39.

When the compressed macro blocks, after error code processing, are input to the decoder which does not operate with video error code, all data in this compressed macro block should be processed as invalid.

FIGURE 38

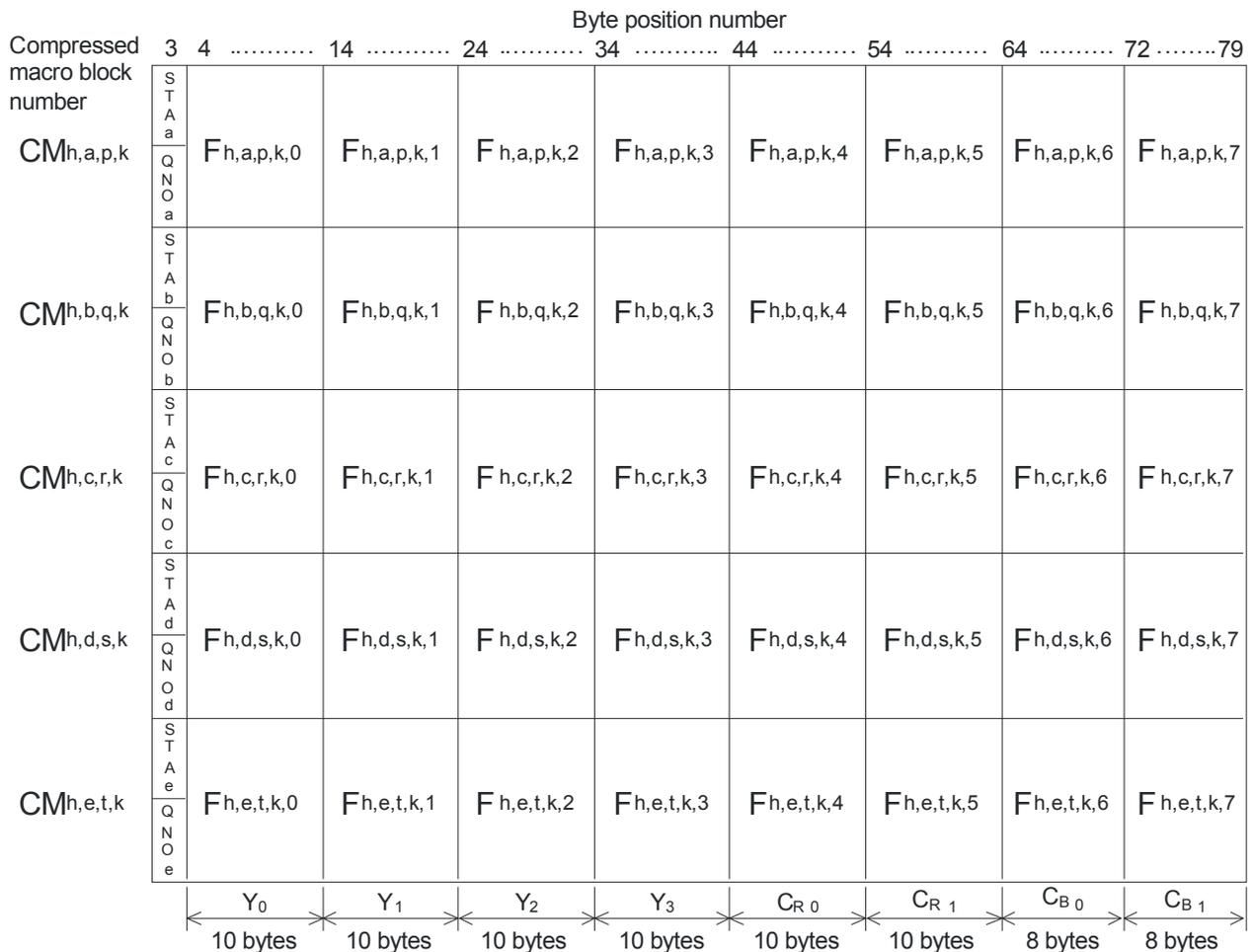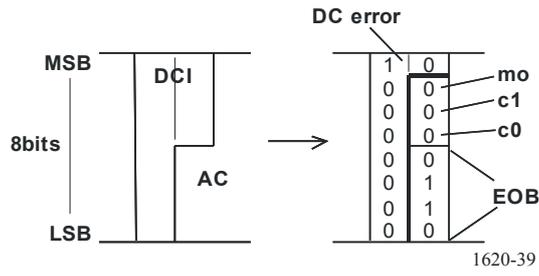**Arrangement of a video segment after the bit rate reduction**

1620-38

FIGURE 39

Video error code

1620-39

Annex 2

Digital filter for sampling-rate conversion

FIGURE 40
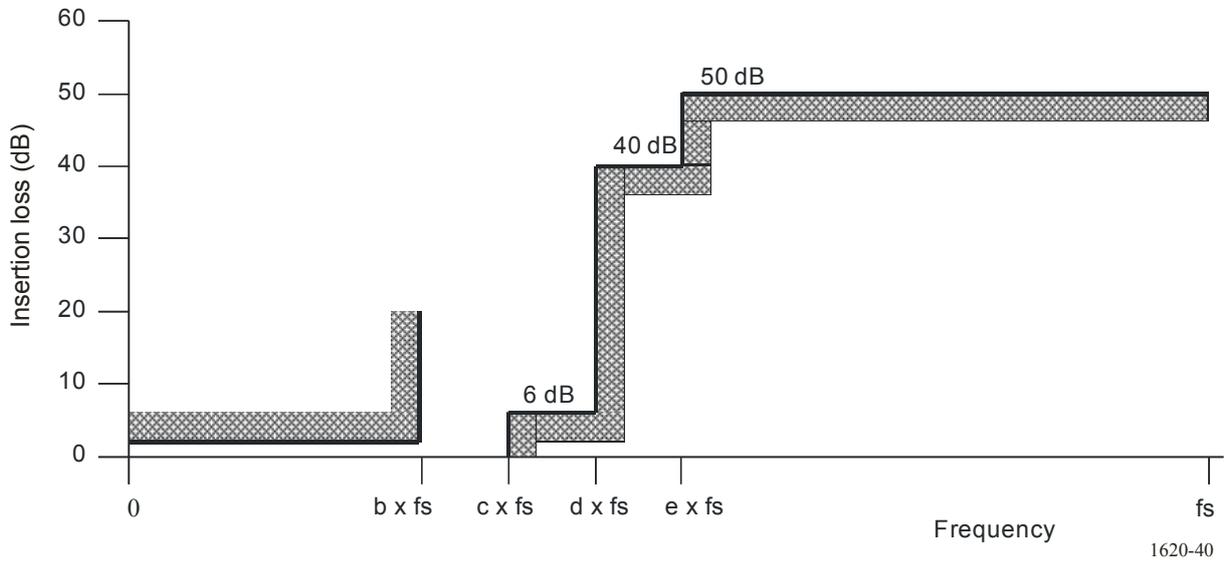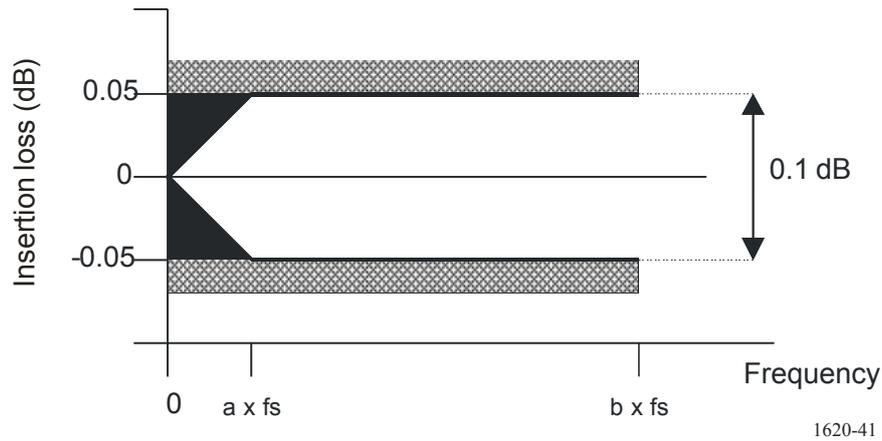
Template for insertion loss frequency characteristic

1620-40

FIGURE 41

Pass band ripple tolerance

1620-41

TABLE 31

Parameter of digital filter

		fs	a	b	c	d	e
1 920 × 1 080/60/I	Y	74.25/1.001 MHz	0.05	0.25	0.333	0.45	0.55
	C_B, C_R		0.025	0.125	0.167	0.225	0.275
1 920 × 1 080/50/I	Y	74.25 MHz	0.05	0.25	0.375	0.50	0.60
	C_B, C_R		0.025	0.125	0.1875	0.25	0.30
1 280 × 720/60 720/60/P	Y	74.25/1.001 MHz	0.05	0.25	0.375	0.50	0.60
	C_B, C_R		0.025	0.125	0.1875	0.25	0.30
1 280 × 720/50/P	Y	74.25 MHz	0.05	0.25	0.375	0.50	0.60
	C_B, C_R		0.025	0.125	0.1875	0.25	0.30

Appendix 1

Bibliography

IEC 61834-2 (1999), Recording – Helical-Scan Digital Video Cassette Recording System Using 6,35 mm Magnetic Tape for Consumer Use (525-60, 625-50, 1125-60 and 1250-50 Systems) – Part 2: SD Format for 525-60 and 625-50 Systems – Part 3: HD Format for 1125-60 and 1250-50 Systems.