



Recommendation ITU-R BT.1363-1
(11/1998)

**Jitter specifications and methods for jitter
measurements of bit-serial signals
conforming to Recommendations
ITU-R BT.656, ITU-R BT.799
and ITU-R BT.1120**

BT Series
Broadcasting service
(television)

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SA	Space applications and meteorology
SF	Frequency sharing and coordination between fixed-satellite and fixed service systems
SM	Spectrum management
SNG	Satellite news gathering
TF	Time signals and frequency standards emissions
V	Vocabulary and related subjects

Note: This ITU-R Recommendation was approved in English under the procedure detailed in Resolution ITU-R 1.

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RECOMMENDATION ITU-R BT. 1363-1^{*,**}**Jitter specifications and methods for jitter measurements of bit-serial signals conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120**

(Question ITU-R 130/6)

(1998-1998)

Scope

This Recommendation provides guidance and tolerances in the measurement of jitter related to the clock stability of serial digital interfaces. Suggested measurement techniques are also made.

The ITU Radiocommunication Assembly,

considering

- a) that many countries have installed digital television production facilities based on the use of serial digital video components conforming to Recommendations ITU-R BT.656, ITU-R BT.799 or ITU-R BT.1120;
- b) that in order to guarantee the operation of such serial digital interfaces specification of jitter parameters and methods to measure jitter is required;
- c) that to implement the above objectives, agreement needs to be achieved in specifying and measuring jitter in bit-serial interfaces conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120;
- d) that the implementation of optical interface for the transmission of signals conforming to draft new Recommendation ITU-R BT.1367 requires the specification of jitter parameters and methods to measure jitter,

recommends

- 1 that where interfaces conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120 are implemented, the jitter should be specified and methods of measuring jitter should be in accordance with the provisions included in Annex 1;
- 2 that compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (e.g. to ensure interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words “shall” or some other obligatory language such as “must” and the negative equivalents are used to express requirements. The use of such words shall in no way be construed to imply partial or total compliance with this Recommendation.

* Radiocommunication Study Group 6 made editorial amendments to this Recommendation in 2003 in accordance with Resolution ITU-R 44.

** Radiocommunication Study Group 6 made editorial amendments to this Recommendation in October 2010 in accordance with Resolution ITU-R 1.

Annex 1

Jitter specifications

1 Introduction

This Recommendation describes techniques for specifying jitter in self-clocking, bit-serial digital systems. It is applicable to sources, receivers, and regenerators.

2 Normative references

There are no normative references associated with this Recommendation.

3 Definitions

3.1 alignment jitter: The variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 input jitter tolerance: Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.3 intrinsic jitter: Jitter at an equipment output in the absence of input jitter.

3.4 jitter: The variation of a digital signal's transitions from their ideal positions in time.

3.5 jitter transfer: Jitter on the output of equipment resulting from applied input jitter.

3.6 jitter transfer function: Ratio of the output jitter to the applied input jitter as a function of frequency.

3.7 output jitter: Jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.8 timing jitter: The variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

3.9 unit interval (UI): Abbreviated UI, it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specifications

Equipment jitter specifications fall into three categories: input jitter tolerance, jitter transfer, and intrinsic jitter. A fourth specification, output jitter, is a network specification and may be used to specify jitter limits at equipment interfaces.

4.1 Input jitter tolerance

Input jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance. Input jitter tolerance is applicable to most serial inputs.

4.1.1 Input jitter tolerance requirements are specified with a jitter template that covers a specified sinusoidal amplitude frequency region (see Fig. 1). This template represents the minimum amount of jitter that the equipment must accept without causing the specified degradation of error

performance. Equipment meeting a jitter tolerance requirement must have an actual jitter tolerance greater than the requirement (see Fig. 2).

4.1.2 Input jitter tolerance requirements are specified with the parameters given in Table 1.

TABLE 1
Input jitter tolerance

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f_1	(Hz)	(Low-frequency specification limit)
f_2	(Hz)	(Upper band edge for A_1 , low-frequency jitter tolerance)
f_3	(Hz)	(Lower band edge for A_2 , high-frequency jitter tolerance)
f_4	(Hz)	(High-frequency specification limit)
A_1	(UI)	(Low-frequency jitter tolerance, f_1 to f_2)
A_2	(UI)	(High-frequency jitter tolerance, f_3 to f_4)
Error criterion		(Criterion for onset of errors)
Test signal		(Test signal used for measurement)

FIGURE 1
Input jitter tolerance template

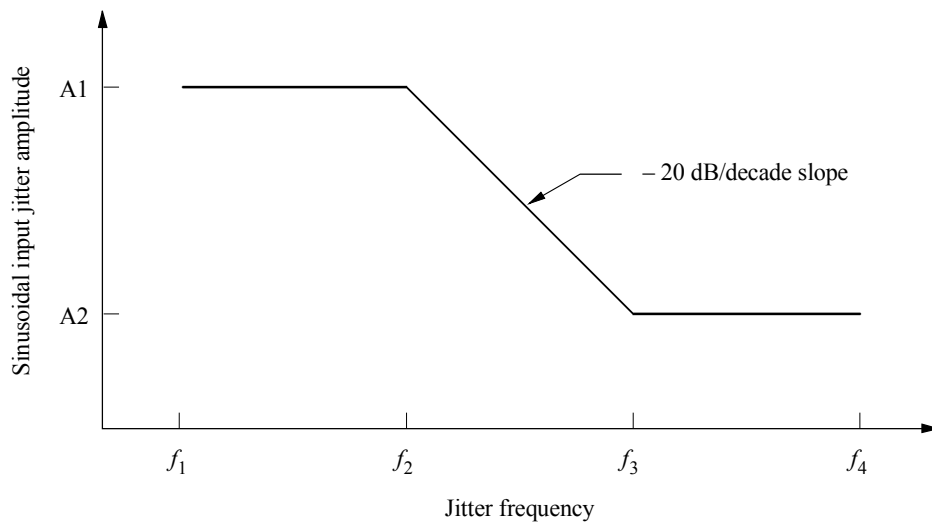
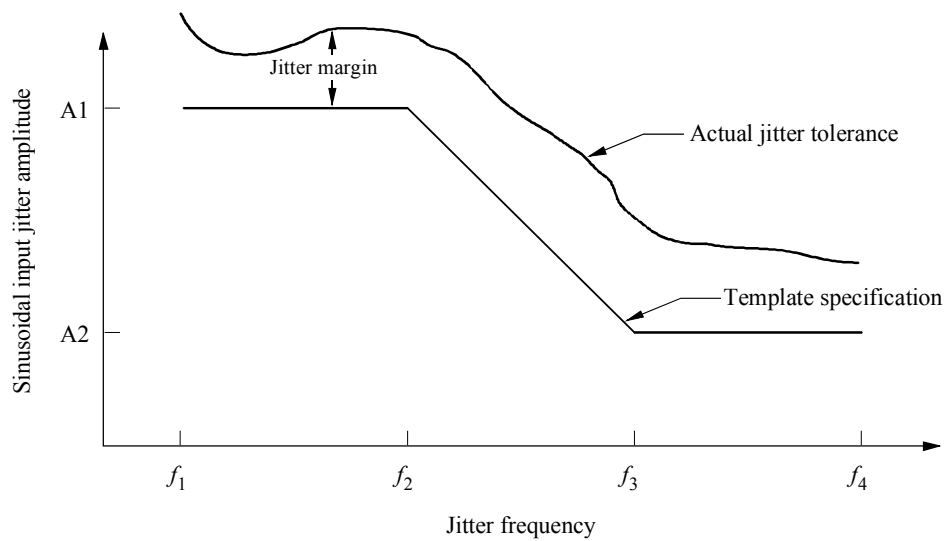


FIGURE 2

Jitter tolerance specification and a compliant jitter tolerance

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4.1.2.1 Frequency band f_1 to f_2 forms the low-frequency jitter tolerance bandpass. At least A_1 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

4.1.2.2 Frequency band f_3 to f_4 forms the high-frequency jitter tolerance bandpass. At least A_2 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

4.1.2.3 A_1 and A_2 shall be specified in UI.

4.1.2.4 The slope of the jitter tolerance requirement between f_2 and f_3 shall be 20 dB/decade. Frequencies f_2 and f_3 are related as follows: $f_2 = f_3/(A_1/A_2)$.

4.1.2.5 The criterion for reaching the onset of errors shall be specified. Either a BER limit or a maximum number of errored seconds over a specified measurement interval should be used.

4.1.2.6 The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

4.1.3 Numerical input jitter tolerance values are provided in the appropriate ITU-R Recommendations which reference this practice. The terminology shall comply with § 4.1.2.

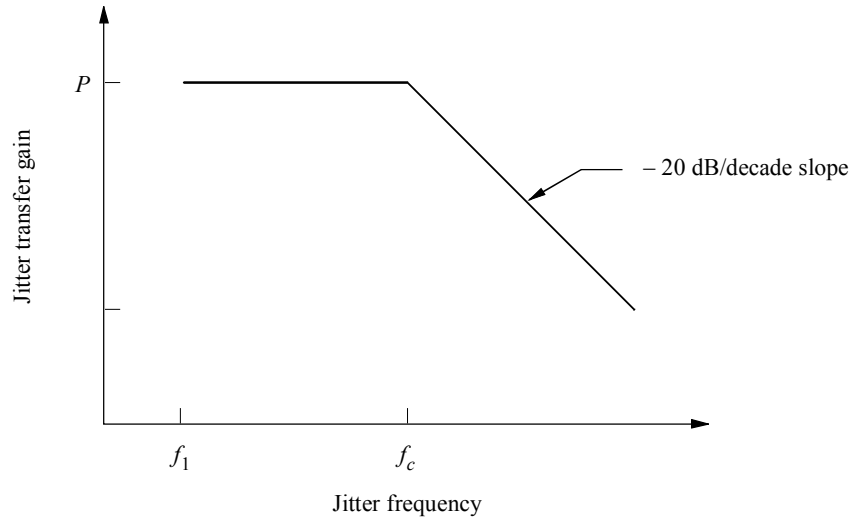
4.2 Jitter transfer

Jitter transfer is jitter on the output of equipment resulting from applied input jitter. Jitter transfer is applicable to a device which produces a serial output from a serial input, such as a regenerator.

Jitter transfer can also occur from reference signals applied to equipment, such as analogue black burst. The jitter transfer templates described below are intended for serial input to serial output jitter transfer.

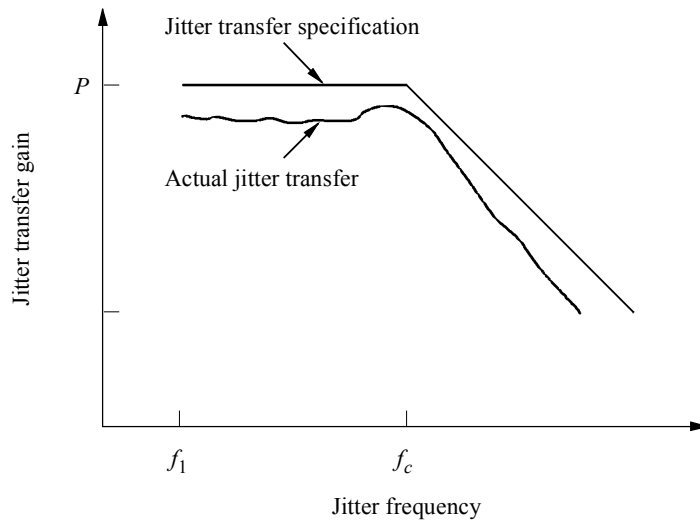
4.2.1 Jitter transfer requirements are specified with a template showing the maximum jitter gain as a function of frequency (see Fig. 3). Equipment meeting a jitter transfer requirement will have a jitter transfer function that lies *within* this template (see Fig. 4).

FIGURE 3
Jitter transfer template



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FIGURE 4
Jitter transfer specification and compliant jitter transfer function



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4.2.2 Jitter transfer requirements are specified with the parameters given in Table 2.

TABLE 2
Jitter transfer requirements

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f_l	(Hz)	(Low-frequency specification limit)
f_c	(Hz)	(Upper band edge of jitter transfer bandpass)
P	(dB)	(Maximum jitter gain, f_l to f_c)
Test signal		(Test signal used for measurement)

4.2.2.1 Frequency band f_l to f_c forms the jitter transfer bandpass. The maximum jitter gain over this bandpass shall be P .

4.2.2.2 From frequency f_c to at least 10 (f_c), the jitter transfer template shall decrease at 20 dB/decade.

4.2.2.3 P shall be specified in decibels.

4.2.2.4 The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

4.2.3 Numerical jitter transfer values are provided in the appropriate ITU-R Recommendations which reference this practice. The terminology shall comply with § 4.2.2.

4.3 Intrinsic jitter and output jitter

Intrinsic jitter and output jitter are both measurements of jitter at an equipment output. They differ in the specification of the input signal to the equipment. Except for this, they are measured identically.

Intrinsic jitter is defined as the amount of jitter at an equipment output when a jitter-free input signal is applied. It is a measure of the amount of jitter generated in the equipment, independent of any jitter transfer. Intrinsic jitter applies to most serial outputs.

Output jitter is the amount of jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input. Output jitter is a network specification, not an equipment specification. Individual equipment should be specified in terms of intrinsic jitter, jitter transfer, and input jitter tolerance. Network interface specifications may use output jitter.

4.3.1 Intrinsic and output jitter shall be specified as peak-to-peak quantities and measured over defined jitter frequency bands. Two measurement bands are specified, one is a subset of the other (see Fig. 5).

4.3.2 Intrinsic and output jitter shall be specified with the parameters given in Table 3.

TABLE 3
Intrinsic and output jitter

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f_1	(Hz)	(Timing jitter, lower band edge)
f_3	(Hz)	(Alignment jitter, lower band edge)
f_4	(UI)	(Upper band edge)
A_1	(UI)	(Timing jitter)
A_2	(s)	(Alignment jitter)
t_m		(Measurement time)
Test signal		(Test signal used for measurement)
n		(Serial clock divider)

4.3.2.1 The timing jitter measurement bandpass is formed by f_1 to f_4 . The maximum peak-to-peak jitter allowed over this bandpass is specified as A_1 .

4.3.2.2 The alignment jitter measurement bandpass is formed by f_3 to f_4 . The maximum peak-to-peak jitter allowed over this bandpass is specified as A_2 .

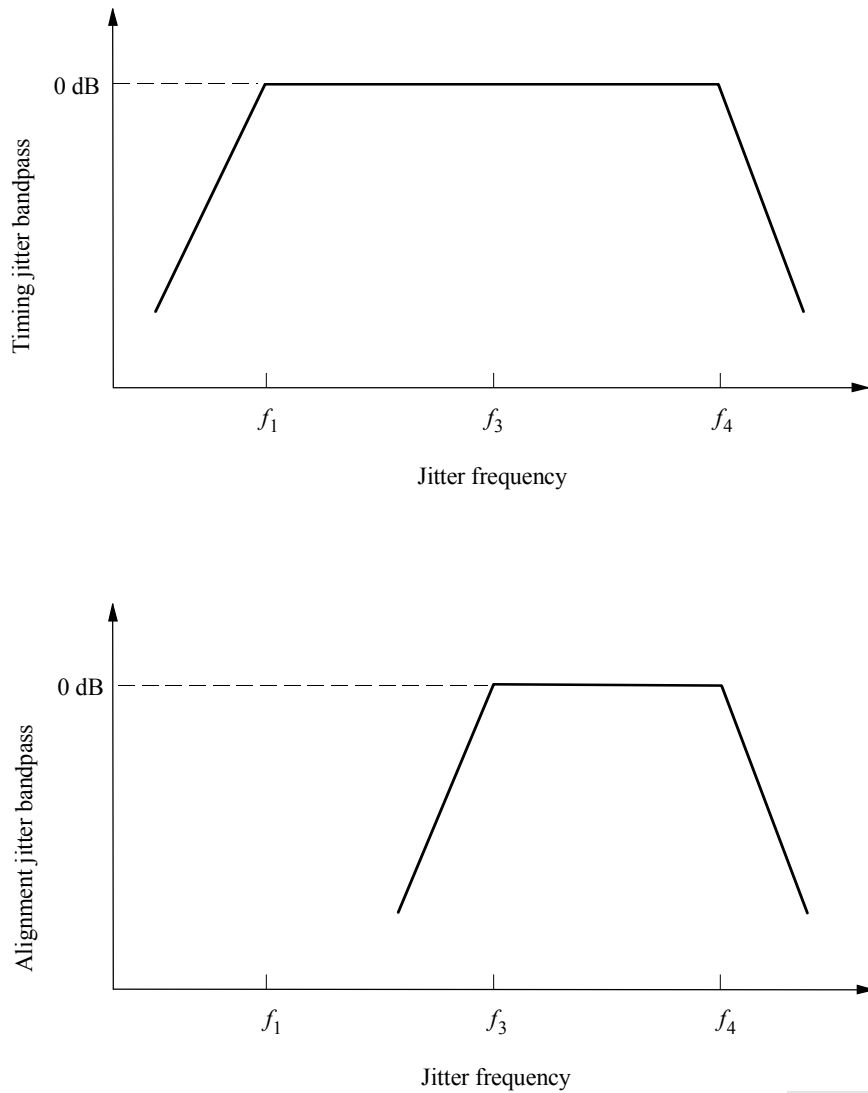
4.3.2.3 A_1 and A_2 shall be specified in unit intervals.

4.3.2.4 Bandpass slopes shall be at least 20 dB/decade and have a minimum phase response unless otherwise specified. Stop band rejection shall be at least 20 dB. Pass band ripple shall be less than +1 dB.

4.3.2.5 A measurement time (t_m) may be specified. If this is omitted, then the measurement time will be determined by the characteristics of the measurement system.

4.3.2.6 The test signal used for the measurement shall be specified. For an intrinsic jitter measurement, the test source jitter shall be negligible compared to the intrinsic jitter specification.

FIGURE 5
Intrinsic and output jitter measurement bandpasses



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4.3.2.7 The serial clock divider, “ n ”, used in the clock extractor should be specified (see Appendix 1 for information on the Clock extractor and clock extractor based measurement methods). The ratio of the serial clock frequency to the clock extractor frequency is “ n ”. It is meaningful for clock extractor jitter measurement methods, but may not be applicable to other measurement techniques.

4.3.3 Numerical intrinsic and output jitter values are provided in the appropriate ITU Recommendations which reference this practice. The terminology shall comply with § 4.3.2.

Appendix 1

Jitter measurement procedures in bit-serial digital interfaces

1 Scope

This Appendix 1 describes methods for measuring jitter performance in bit-serial digital interfaces.

1.1 Introduction

Jitter is one of the most important parameters in the performance of serial digital transmission systems. It can cause errors in the transmission and recovery of digital data, and may degrade analogue signal performance if the jitter is transferred through the digital-to-analogue conversion process. Characterizing and measuring jitter are important for reliable and predictable serial digital system operation.

2 Informative references

3 Definitions

3.1 alignment jitter: Variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 clock extractor: A device which is able to extract the serial data clock from a serial data stream, and outputs a clock-related trigger. It may also provide the serial digital data reclocked with the extracted clock.

3.3 DSO: Acronym for digital storage oscilloscope.

3.4 DUT: Acronym for device under test.

3.5 error rate tester: A device that quantifies the error rate of a serial digital signal. Two examples are the classic bit error rate (BER) tester and the field rate CRC method (EDIT) described in Recommendation ITU-R BT.1304.

3.6 input jitter tolerance: Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.7 intrinsic jitter: Jitter at an equipment output in the absence of input jitter.

3.8 jitter: Variation of a digital signal's transitions from their ideal positions in time.

3.9 jitter generator: A device which produces a serial digital signal containing sinusoidal jitter of adjustable amplitude and frequency.

3.10 jitter receiver: Demodulates and allows measurement of the jitter present on a serial signal. It commonly provides an output proportional to the demodulated jitter.

3.11 jitter transfer: Jitter on the output of equipment resulting from applied input jitter.

3.12 jitter transfer function: Ratio of the output jitter to the applied input jitter as a function of frequency.

3.13 output jitter: Jitter at the output of equipment that is embedded in a system network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.14 phase demodulator: A device that provides as its output a signal proportional to the phase difference of two input signals.

3.15 SDI: Acronym for Serial Digital Interface, typically referring to Recommendation ITU-R BT.656 system.

3.16 timing jitter: Variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

3.17 unit interval (UI): The period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specification

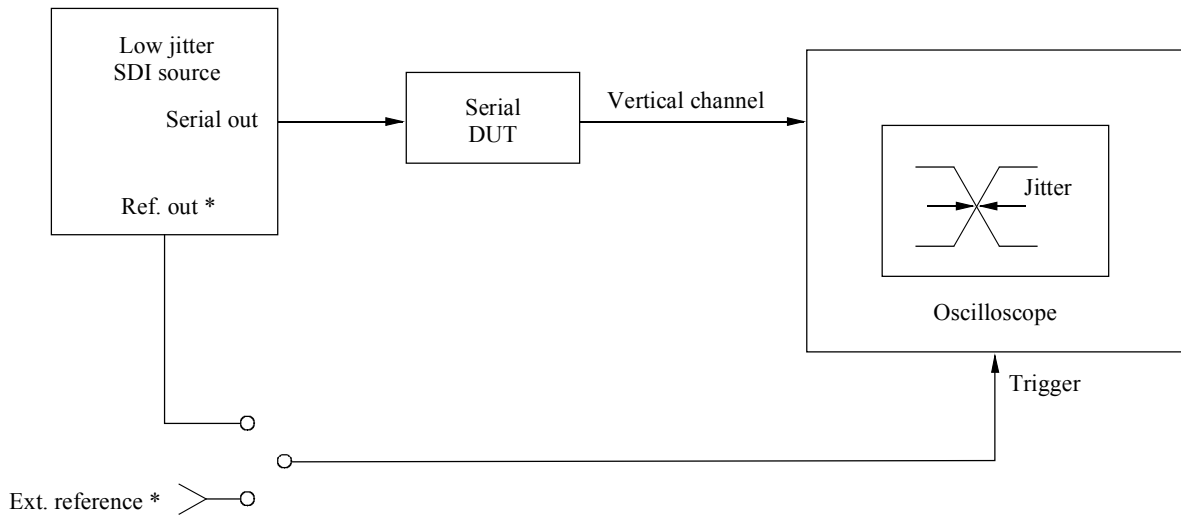
Four methods are described: The first uses an available reference clock to trigger an oscilloscope; the second uses a clock extractor with defined characteristics to trigger the oscilloscope; the third and fourth are based on a phase demodulator method jitter receiver.

4.1 Oscilloscope measurement by means of triggering on a reference signal

If a reference signal is available, a basic jitter measurement can be done (see Fig. 6). The oscilloscope is directly triggered by the reference signal. This reference signal could also be a serial digital signal with high stability, for example, for a 270 Mbit/s ITU-R BT.656 signal, the 27 MHz parallel clock, the 270 MHz serial clock or an ITU-R BT.656 serial signal. The digital data signal is connected to the suitably terminated vertical channel of the oscilloscope and an eye measurement is done. The jitter is typically measured at the eye crossing.

- Presentation of measurement results: The test signal, the jitter amplitude, the parameters of the oscilloscope (bandwidth, etc.), and the measurement time should be indicated.
- Background information: This measurement procedure provides a coarse survey of jitter in an SDI signal. The measurement result depends on the stability of the reference signal (its jitter sets the measurement floor), the type of oscilloscope, and the measurement time (e.g., when a DSO is used in persistence mode). All of these parameters influence the measurement result and contribute to variability in the result as conditions vary. This method does not allow bandwidth restriction as generally required in jitter specification. This method is not recommended if other jitter measurement methods are available.

FIGURE 6
Oscilloscope jitter measurement by means of a reference signal



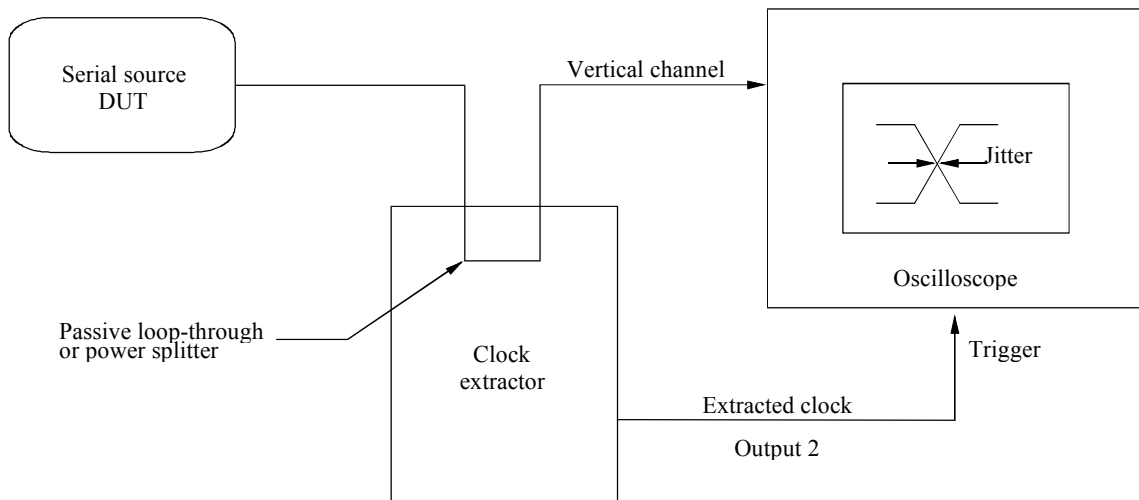
* A for a 270 Mbit/s ITU-R BT.656 signal, the 27 MHz parallel clock, the 270 MHz serial clock or a ITU-R BT.656 signal.

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4.2 Jitter measurement by means of a clock extractor

The jitter in a signal output can be measured by using a device to extract clock and then trigger an oscilloscope or other indicating device (see Fig. 7).

FIGURE 7
Jitter measurement less than 1 UI using a clock extractor



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4.2.1 Clock extractor block diagram

The clock extractor typically consists of a wideband clock recovery circuit followed by a second, narrow band PLL (see Fig. 8). This second PLL can be set to two different loop bandwidths, so that two different jitter transfer functions are available (see Fig. 9). Clock output 2 is used to trigger the indicating device. The clock extractor shall have the following characteristics:

1. It shall be capable of being put in series with the signal output and provide enough signal for the indicating device. It shall not modify the output signal characteristics in ways that obscure or modify the jitter on the signal.
2. To measure timing jitter (A_1), the clock extractor shall have a clock recovery bandwidth of f_1 . To measure alignment jitter (A_2), the clock extractor shall have a clock recovery bandwidth of f_3 (see Fig. 9).
3. The jitter transfer function of the clock extractor shall roll-off at 20 dB/decade or greater and have a minimum phase response unless otherwise specified. Ripple within the pass band shall be less than +1 dB (see Fig. 9).
4. The extracted clock frequency shall be the serial clock frequency divided by “ n ”, where “ n ” is defined in § 4.3.2 of the body of this Recommendation.
5. The clock extractor may have an optional clock output 1, which has a clock recovery bandwidth for greater than or equal to f_3 . It is preferable that for equal f_4 .

4.2.2 Indicating device specifications

The indicating device used to observe the jitter shall have the following characteristics:

1. The horizontal and/or trigger bandwidth of the indicating device shall not attenuate the observed jitter. The trigger bandwidth shall be at least f_3 .
2. The indicating device shall not create intersymbol interference at the zero-crossing point. This requires a vertical system step response that transitions and settles in less than 1 UI.
3. The indicating device shall acquire sufficient samples so that peak-to-peak jitter can be determined. This requires sampling until the shape of the jitter distribution is known. If the jitter specification includes a measurement time, this shall be the minimum acquisition time. The maximum acquisition time will depend on the device sample rate and the type of jitter distribution. For example, a sinusoidal distribution will typically be determined with fewer samples than will a Gaussian-like distribution.

NOTE – The minimum required measurement time depends on how quickly the measurement device collects samples. For digital storage oscilloscopes (DSOs), this is determined by the acquisition rate and the number of samples per acquisition. While the latter term is related to the advertised DSO sample rate, the former is not. DSOs with identical sample rates may take very different amounts of time to build a sufficient sample record to make a measurement.

The minimum measurement for a given oscilloscope may be determined as follows: first, have the scope acquire for a very long time to establish the jitter level. Then, successively shorter measurements are taken until the results start showing unacceptable error or variation. This establishes the minimum measurement time for the scope. Experienced users often have an intuitive feeling for this value based on how the sample distribution is filling in.

4. If the indicating device is an oscilloscope, the jitter measurement is usually made at the eye crossing. A digital storage oscilloscope with infinite persistence is recommended.

FIGURE 8
Clock extractor block diagram

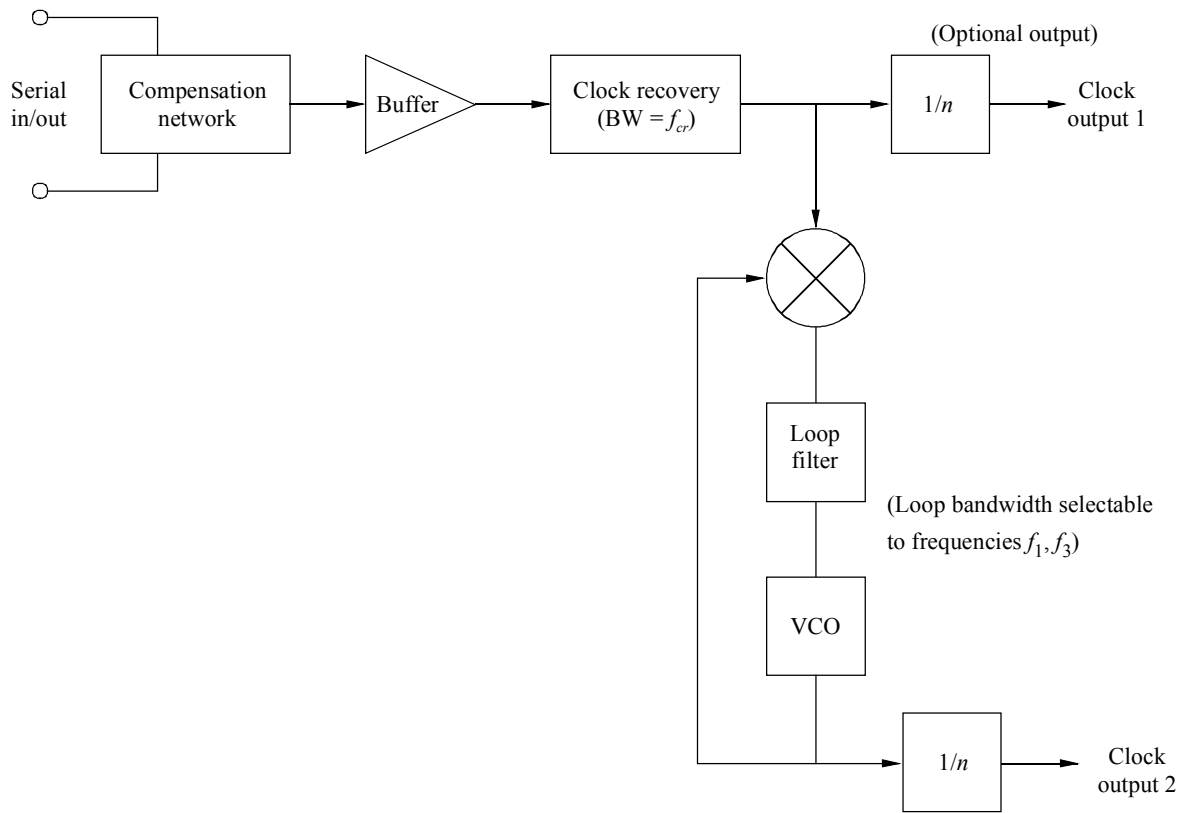
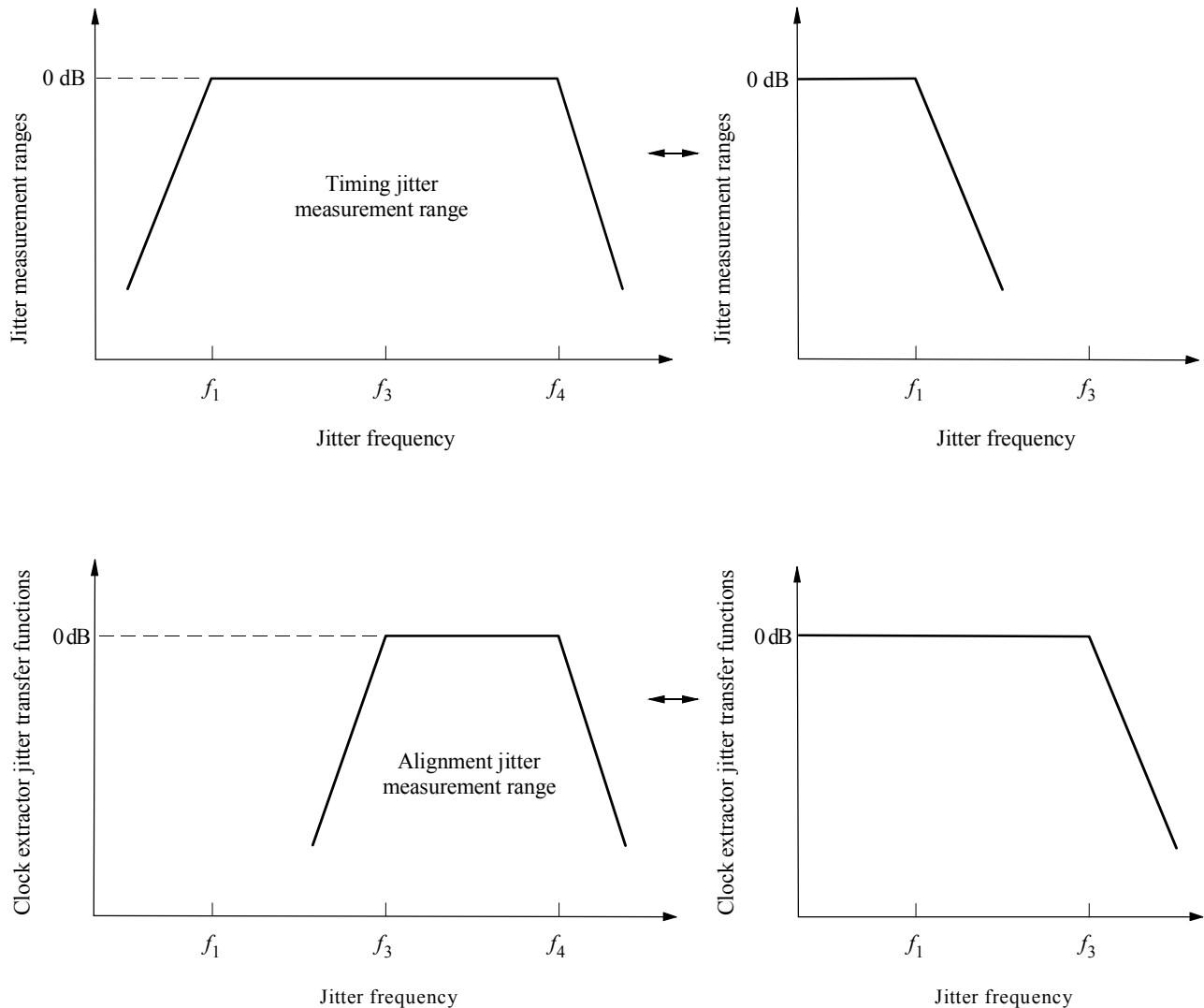


FIGURE 9

Jitter measurement bandwidth and corresponding clock extractor jitter transfer function



1363-09

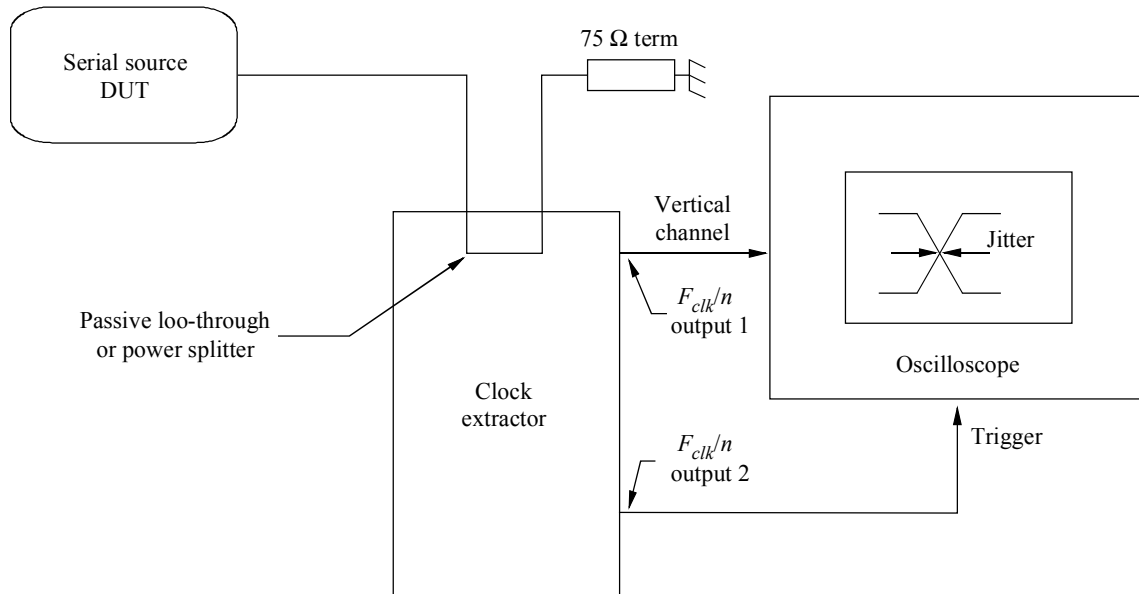
4.2.3 Measurement of timing jitter

The clock extractor is set to bandwidth f_1 . The clock output 2 is connected to the trigger channel of the oscilloscope. The signal connected to the oscilloscope vertical channel depends on the jitter amplitude being measured. For jitter amplitudes less than 1 UI, the loop-through signal is used (see Fig. 7). For jitter amplitudes greater than 1 UI, two different connections are possible:

1. (Preferred) If the clock extractor has a clock 1 output (Fig. 8), this signal is applied to the oscilloscope vertical channel (see Fig. 10). This connection will ensure jitter between frequencies f_1 and f_c , where f_c is the bandwidth of the wideband clock recovery circuit.
2. If the clock extractor has simultaneous outputs at bandwidths f_1 and f_3 , one output is connected to the vertical channel and the second to the trigger. This connection measures jitter between frequencies f_1 and f_3 .

- Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.

FIGURE 10
Measuring jitter greater 1 UI using a clock extractor and an oscilloscope



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4.2.4 Measurement of alignment jitter

The clock extractor is set to bandwidth f_3 . The clock output 2 is connected to the trigger channel of the oscilloscope. The loop-through signal is connected to the oscilloscope vertical channel (see Fig. 7).

- Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.

4.2.5 Phase noise measurement by means of a clock extractor

This clause describes a simple method for making a phase noise measurement on the extracted clock using a spectrum analyser. This technique allows an examination of the side bands of the clock signal, which correspond with the jitter frequencies in the SDI signal (see Fig. 11).

The output 1 of the clock extractor is connected to a spectrum analyser. The spectrum analyser is switched to phase noise measurement and the phase noise of the clock under test is examined.

- Presentation of measurement results: The test signal, the clock extractor PLL bandwidth, the resolution bandwidth and span of the spectrum analyser, and a plot of the spectrum should be indicated.

4.3 Jitter measurements using a phase demodulator

Jitter can be conveniently observed and measured if the phase modulation sidebands are heterodyned down to D.C. One popular method is to recover two clocks from the signal, one with a very wide clock recovery bandwidth and the second with a narrow bandwidth, and apply them to a phase demodulator (see Fig. 12). The output signal is then applied through selectable bandpass filters to a peak reading voltmeter. The output can also be applied to a spectrum analyser to observe the jitter frequency terms (see Fig. 13). Jitter receivers typically use the phase demodulator method.

4.3.1 A jitter receiver shall be capable of measuring peak-to-peak jitter over the jitter measurement bandpasses described in § 4.3.2 of the body of this Recommendation.

4.3.2 The jitter spectrum can be observed by connecting the phase demodulator output to a spectrum analyser or an oscilloscope with fast Fourier transform (FFT) option (see Fig. 13).

Presentation of measurement results: The test signal, measurement time, measured jitter level and measurement bandpass, and a description of the measurement equipment should be documented.

FIGURE 11
Jitter measurement by means of a clock extractor and a spectrum analyser

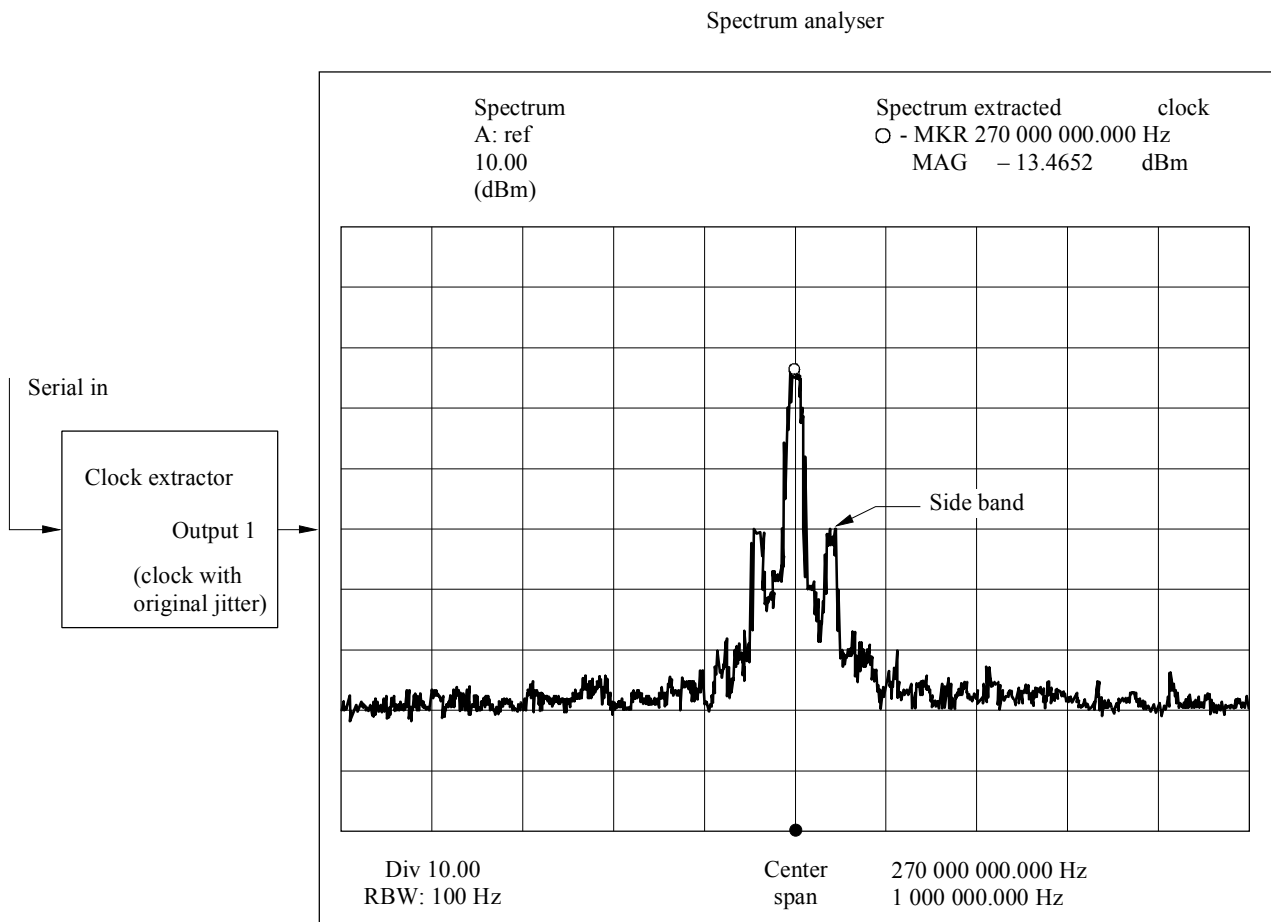
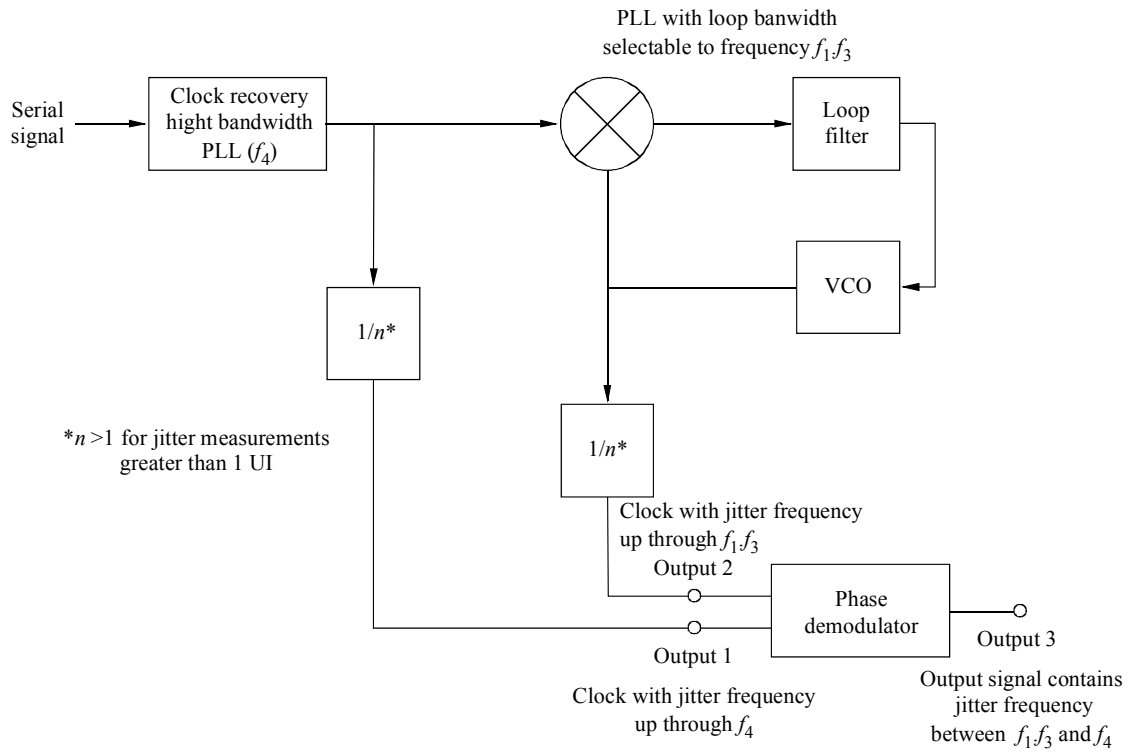
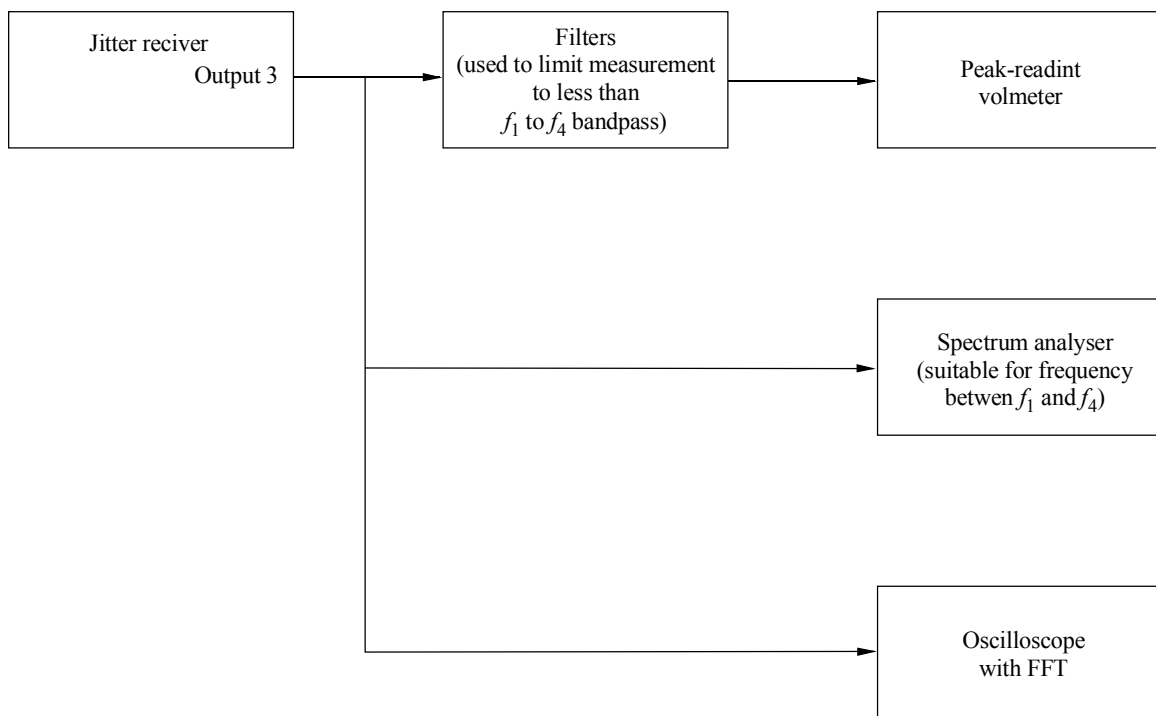


FIGURE 12
Block diagram of a jitter receiver
 (clock extractor high-quality PLL, demodulator)



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FIGURE 13
Jitter receiver output connections



1363-13

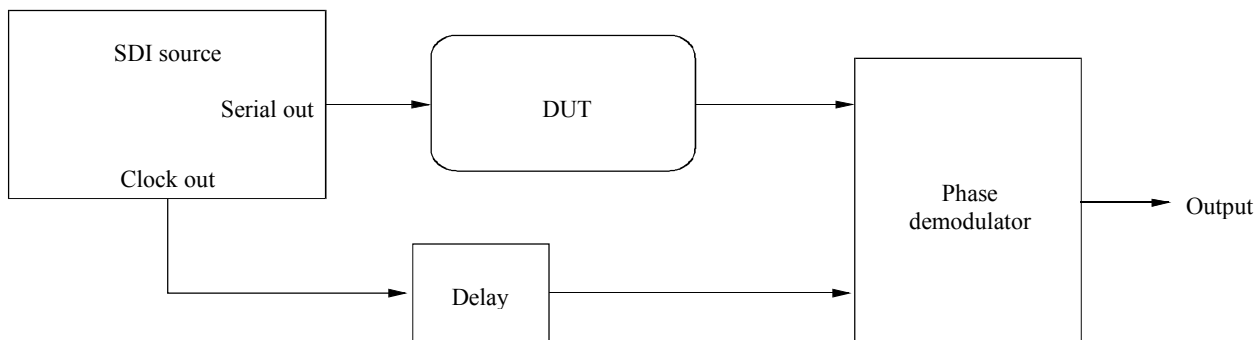
4.4 Phase demodulator measurement with an available reference signal

If a reference signal is available, then a demodulated jitter measurement may be made using the set-up shown in Fig. 14. The reference and data signals are connected to the two inputs of a digital phase demodulator. The output of the demodulator may be processed in several ways. The output may be filtered to establish the lower and upper band edges and then passed to an oscilloscope for display of the jitter results (note that the vertical scale of the oscilloscope now represents the jitter amplitude). Alternatively, the demodulated jitter waveform may be captured and then digitally filtered to establish the upper and lower band edges. Finally, the jitter spectrum may be obtained either by performing an FFT on a captured waveform, or by connecting the demodulator output to a spectrum analyser.

- Presentation of measurement results: The test signal type, the upper and lower band edges, the measurement time, and the peak-to-peak jitter amplitude should be recorded.
- Background information: This measurement method is sensitive to any pattern dependent jitter introduced by the phase detector in the jitter demodulator. The phase detector shall be of a type to avoid introducing pattern dependent jitter. The method also requires that the phase demodulator be calibrated so that the vertical indication on the oscilloscope may be related to the jitter amplitude. This may be accomplished by providing a frequency shift between the reference and the data signal and noting the slope of the phase demodulator output. Finally, this technique is only able to resolve jitter less than 1 UI in magnitude in the limit, and in practice less than 1 UI because of nonlinearities in the demodulator transfer function near the limits of its range.

FIGURE 14

Phase demodulator measurement with an available reference signal



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5 Jitter tolerance measurement

Jitter tolerance measurements require a calibrated jitter generator and an error rate measurement device (see Fig. 15).

- Procedure

Step 1: Connect the equipment as shown in Fig. 15. With the generator jitter amplitude set to 0 UI pp, verify error-free operation.

Step 2: Set the generator jitter frequency as desired, and increase the jitter amplitude until the onset of errors criterion is reached. Note the jitter amplitude and frequency:

Step 3: Repeat Step 2 for a sufficient number of frequencies to determine the jitter tolerance curve.

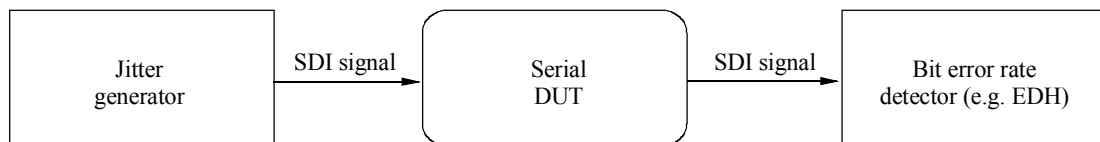
– To verify compliance with a jitter tolerance template:

Step 1: Set the jitter amplitude and frequency to a template point. Verify that the onset of errors criterion is not reached.

Step 2: Repeat Step 1 for a sufficient number of template points between frequencies f_1 and f_3 . Template form is described in the body of this Recommendation.

NOTE – A calibrated jitter receiver can be used to establish the jitter amplitude of an uncalibrated jitter generator.

FIGURE 15

Jitter tolerance measurement

1363-15

6 Jitter transfer measurement

Jitter transfer measurements require a calibrated jitter generator and a calibrated jitter receiver (see Fig. 16). An enhanced method requires a jitter generator with an external jitter input, a jitter receiver, and a spectrum analyser with a tracking oscillator output (see Fig. 17).

– Basic technique:

Step 1: Perform a jitter tolerance measurement of the DUT over the desired frequency range.

Step 2: Connect the equipment as shown in Fig. 16. Set the jitter generator level so that it is less than the measured jitter tolerance over the band of interest, yet large enough for good measurement accuracy.

Step 3: Note the jitter receiver reading and the jitter frequency.

Step 4: Divide the jitter receiver reading by the jitter generator level to obtain the jitter gain at this frequency.

Step 5: Repeat Step 3 for a sufficient number of frequencies to determine the jitter transfer function.

NOTE – If the jitter generator or the jitter receiver frequency response is not flat, connect the generator and receiver directly together to establish a deviation table.

– Enhanced technique:

Step 1: Perform a jitter tolerance measurement of the DUT over the desired frequency range.

Step 2: Connect the equipment as shown in Fig. 17, bypassing the DUT. Verify linear, error-free operation of the jitter receiver.

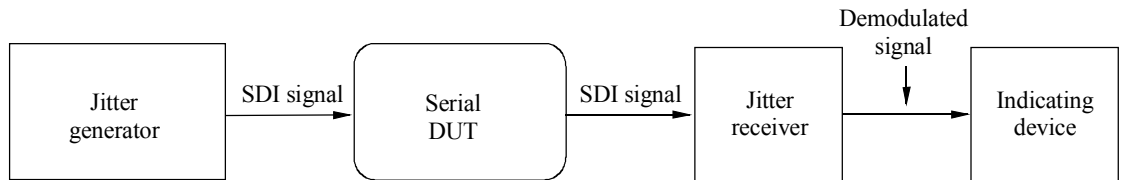
Step 3: Set the tracking generator output amplitude so that the jitter generator level is less than the measured jitter tolerance over the desired frequency range. Select an appropriate resolution bandwidth on the spectrum analyser. Save the trace on the analyser.

Step 4: Connect the DUT. Subtract the stored trace from the display trace. The difference is the DUT jitter transfer function.

NOTE – A network analyser can be used in place of the spectrum analyser and tracking generator combination. A vector network analyser permits measurement of both the phase and magnitude of the jitter transfer function.

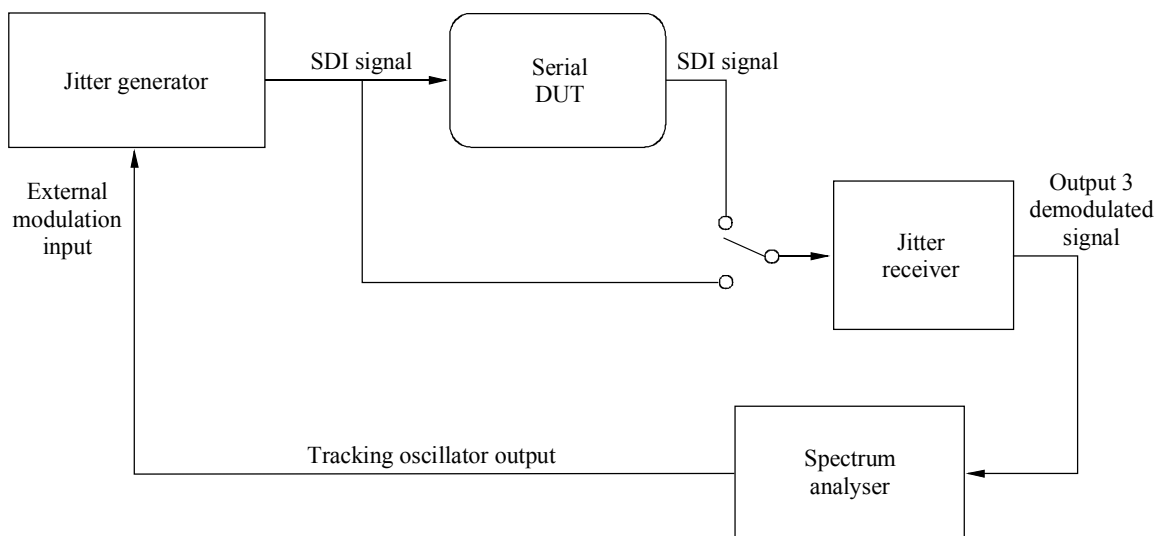
To verify compliance with a jitter transfer template: Using either the basic or enhanced technique, verify that the jitter transfer is less than the template requirement, from f_1 to $10(f_c)$.

FIGURE 16

Jitter transfer function measurement (basic method)

1363-16

FIGURE 17

Jitter transfer function measurement (enhanced method)

1363-17

Appendix 2

Jitter characteristics and measurement for bit-serial digital studio interfaces

Introduction

Transferring digital signals from one location to another involves converting the signals into an analogue physical representation at the sending end and then interpreting that representation to extract the data at the receiving end. This is necessary because any signals that are physically represented inherently have analogue properties. These properties include the levels and timing of the data intervals and the transitions between them, the spectral distribution that results, and any signal distortions that occur in the transmission system. This is true whether the signals are modulated onto an RF carrier or transmitted directly as data using an appropriate form of encoding. Analogue effects that can alter digital signals are attenuation, spectral roll-offs and anomalies, overshoots, undershoots, time dispersion, and jitter. The first several are frequency- and amplitude-related effects while jitter is the sole timing-related disturbance.

1 Scope

This guideline examines the types of jitter in directly transmitted data signals, the methods for measuring each one, and some of the impacts they can have on system operation. Additionally, some of the system design approaches that can minimize or mitigate the impact of jitter are presented.

2 Jitter definition

In this guideline, the 270 Mbit/s (Mb/s) serial digital interface (SDI) signals of Recommendation ITU-R BT.656 will be used as an example, but the same concepts apply to serially transmitting everything from 3.1 Mbit/s AES-3 audio data streams through 1.5 Gbit/s HDTV versions of the SDI. Only the numerical values used for equipment specifications and measurements change when covering this large range of digital signals.

To send digital data streams from one place to another over a single wire or fibre, data is encoded using one of several self-clocking methods. These include such schemes as NRZ, NRZI, AMI, block coding, bi-phase mark, and others which typically trade-off the resulting data signal bandwidth and spectral shaping for ease of clock extraction, error detection ability, or other performance features. The important thing about all of these designs is that they allow the clock to be extracted from the data stream so it can be used to recover the data.

Clocking information is usually extracted using phase lock loop circuits. The transition locations in a data stream are instantaneously compared with transitions of a synthesized clocking signal coming from a local oscillator (typically an RC- or LC-type voltage controlled oscillator) at the receiver. The local clock's frequency is then adjusted up or down until the extracted clock's edges agree with the incoming data edges. This process is straightforward as long as the data transitions occur at the expected intervals; that is, integer multiples of the serial clock period. In real systems, however, the data transitions will deviate somewhat from their ideal position; that is, the pulse positions vary with respect to a high stability frequency-locked clock. This unwanted pulse position variation is jitter.

Jitter is defined as the variation of a digital signal's significant instants (such as transition points) from their ideal positions in time. Jitter can cause the recovered clock and the data to become momentarily misaligned in time. Data may be misinterpreted (latched at the wrong time) when this misalignment becomes great enough.

Jitter is measured in terms of the unit interval (UI), which represents the period of one clock cycle and, for NRZ or NRZI encoded data, corresponds to the nominal minimum time between transitions of the serial data. This can be seen in Fig. 18a), where the data of an NRZI signal and the related clock ticks are shown. Fig. 18b) shows the effect of jitter on the midpoint crossings of the data transitions, as would be seen on an eye-pattern presentation (repetitive display of transition points overlaid upon one another). Increasing jitter closes the eye in the time dimension and makes decisions between data states correspondingly more difficult, just as signal voltage noise does in the amplitude dimension.

Jitter, then, can be thought of as the phase variation (or modulation) of the serial data stream. This phase modulation has a spectrum that corresponds to the frequency with which the data's clock is modulated. Thus, it is possible to plot an amplitude versus frequency characteristic of the jitter. For example, in Fig. 19, a single spike at 6 144 Hz indicates the presence of sinusoidal phase variation (jitter) at a rate of 6 144 Hz. The amplitude of the spike would indicate how much of the data eye was closed.

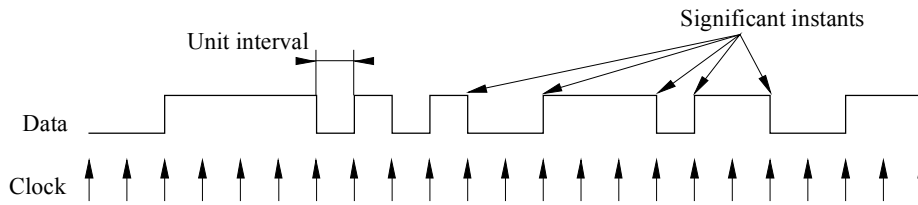
3 Classes of jitter

Absolute jitter is the aggregate of all jitter frequency components found in a signal, from very low to very high frequency. Measuring exact absolute jitter is practically impossible because it is difficult to generate an absolute reference defining where data edges should be. The practical study of jitter divides it into three classes, based on the frequency content of the jitter modulation.

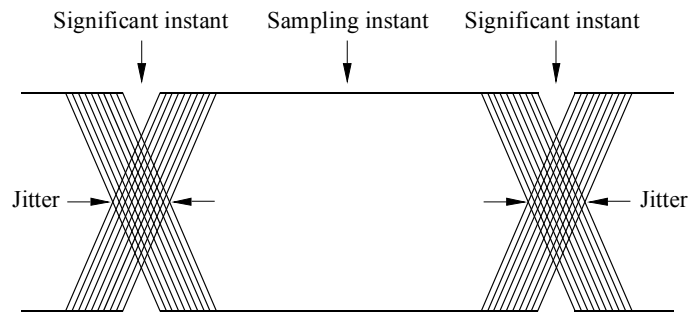
The very lowest frequency variations in the positions of a signal's transitions are termed wander. Wander typically has no effect on the capability of the clock extraction and decoding electronics to accurately recover the digital data stream because this low-frequency variation can be followed by the PLL (unless the wander causes the data rate to go outside the range of the controlled reference oscillator).

FIGURE 18

Elements of serial data signals and relationships to jitter



a) Relationship of data and clock for SDI signals showing unit interval and significant instants

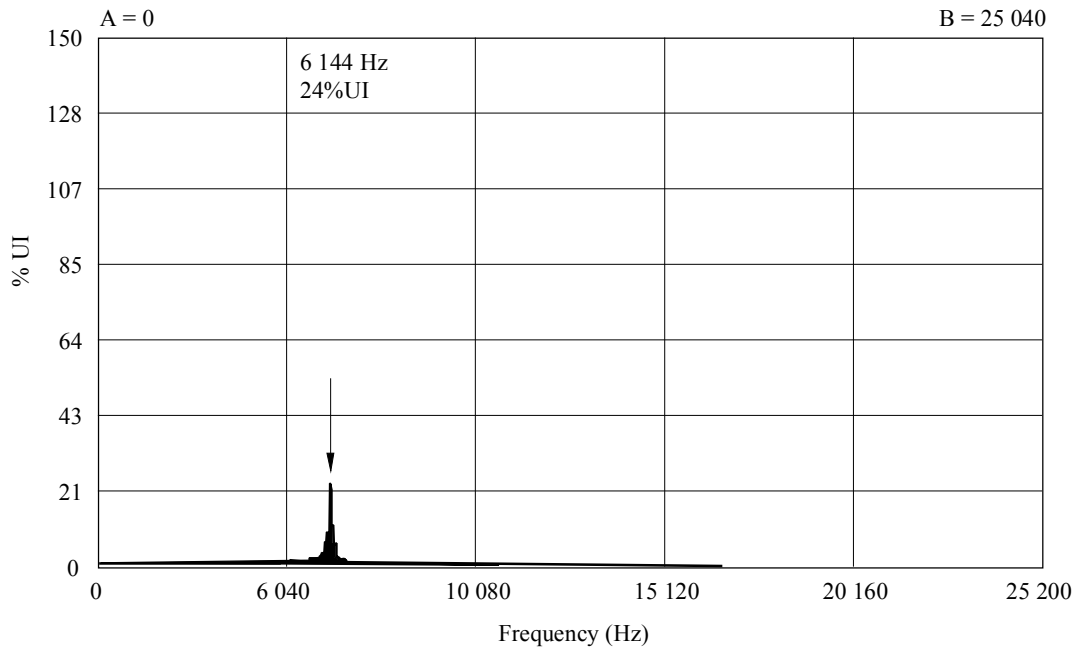


b) Eye pattern showing jitter at significant instants

1363-18

Wander may, however, cause problems in later down-stream processing. Wander is generally defined as jitter with frequency components below a particular frequency. In SDI applications, this assigned cutoff is 10 Hz. Measuring wander and absolute jitter implies that the clocking reference used to identify edge jitter be extremely stable with no jitter component of its own. Typical PLL-extracted clocks are unsuitable for this measurement. The source of such an accurate reference signal might be a high-Q crystal oscillator; however, access to this type of signal is not common in SDI applications. This limitation typically causes wander to be excluded in jitter measurements.

FIGURE 19
Jitter frequencies

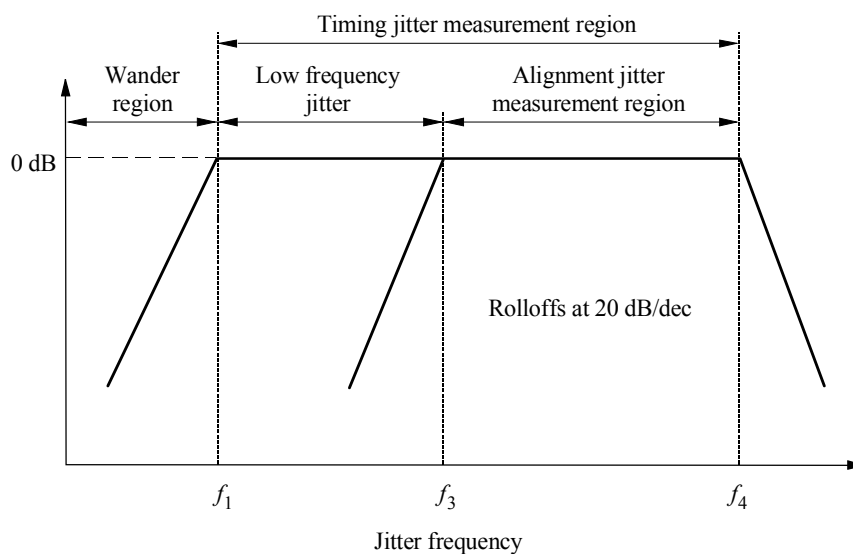


$F = -65\,536$ Hz, Resol = 16.00 Hz, Bias = Amplitudes, Band = 10 Hz, Delta Cursor = 25 040, C = 0

1363-19

Jitter that occurs above the highest frequency defined as wander is termed timing jitter. Jitter that is measured relative to a recovered clock with a loop bandwidth defined by f_3 (Fig. 20) is called alignment jitter. The difference between timing jitter and alignment jitter is the low-frequency jitter.

FIGURE 20
Jitter measurement regions



1363-20

The timing jitter measurement is used to provide an idea of how the overall system is performing. It can be measured by setting the loop filter bandwidth of the clock recovery system to f_1 . The result will include all frequencies of jitter above the loop filter cutoff to the upper limit of the measurement. This broadband measurement will not specifically identify jitter that could cause data recovery errors.

Alignment jitter can provide information on jitter that directly affects the receiver's ability to properly recover data. This type of error occurs because the PLL is not able to track the timing changes of the incoming signal. If the timing errors become large enough, the decoder will "slip" a bit, which will cause an error in the decoded data. This produces a word framing error, which will not be corrected until the next timing reference signal.

Low-frequency jitter generally does not cause problems in the serial link. Large amounts of low-frequency jitter can be tolerated by the serial link, as the PLL follows these timing changes and maintains proper data recovery. However, one must be aware of this band of jitter, as it will be present in the recovered parallel clock. This parameter is important to monitor if the recovered clock is to be used as a reference signal in the parallel domain.

The low-frequency jitter can be found by subtracting the alignment jitter from the timing jitter. This will yield accurate results for most types of jitter, such as sinusoidal or random sources of jitter. If the jitter source is a complex waveform, such as a square wave, the frequency and duty cycle will have an effect on this calculation.

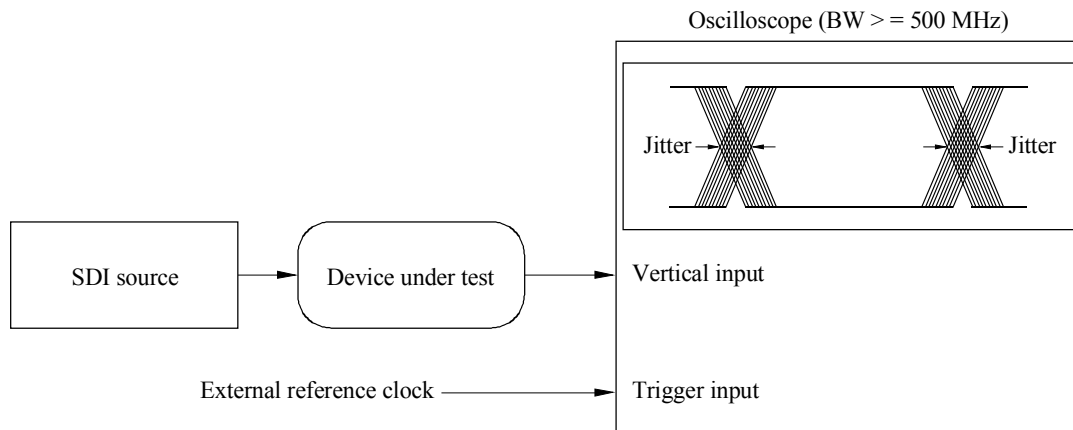
In the case of Recommendation ITU-R BT.656 – Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601, the frequency roll-off definition for alignment jitter measurements (f_3) is 1 kHz. Because there are many popular SDI receivers already in use throughout the industry, this value had to be chosen to be useful for all systems. When choosing this number, a frequency high enough to ignore jitter from typical genlock circuits (200 Hz or greater) and low enough to include the clock recovery bandwidths for all popular receiver integrated circuits (10 kHz or less) had to be found.

4 Jitter measurements

Several different instruments and connection arrangements can be used to measure jitter of various types. The more complex techniques will produce more informative results, but the simpler methods can be meaningful as a starting point for understanding the jitter types occurring in a particular system.

The simplest method for observing and measuring jitter is the use of an oscilloscope with an external reference for triggering, as shown in Fig. 21. The SDI source and the external reference must be locked to a common clock, as any frequency difference (which is not jitter) may interfere with the measurement. The spread of the crossing points of an eye display will reveal the jitter amplitude. If a highly stable external reference, such as a clock derived from black burst, is used, absolute jitter, including wander, will be displayed.

FIGURE 21

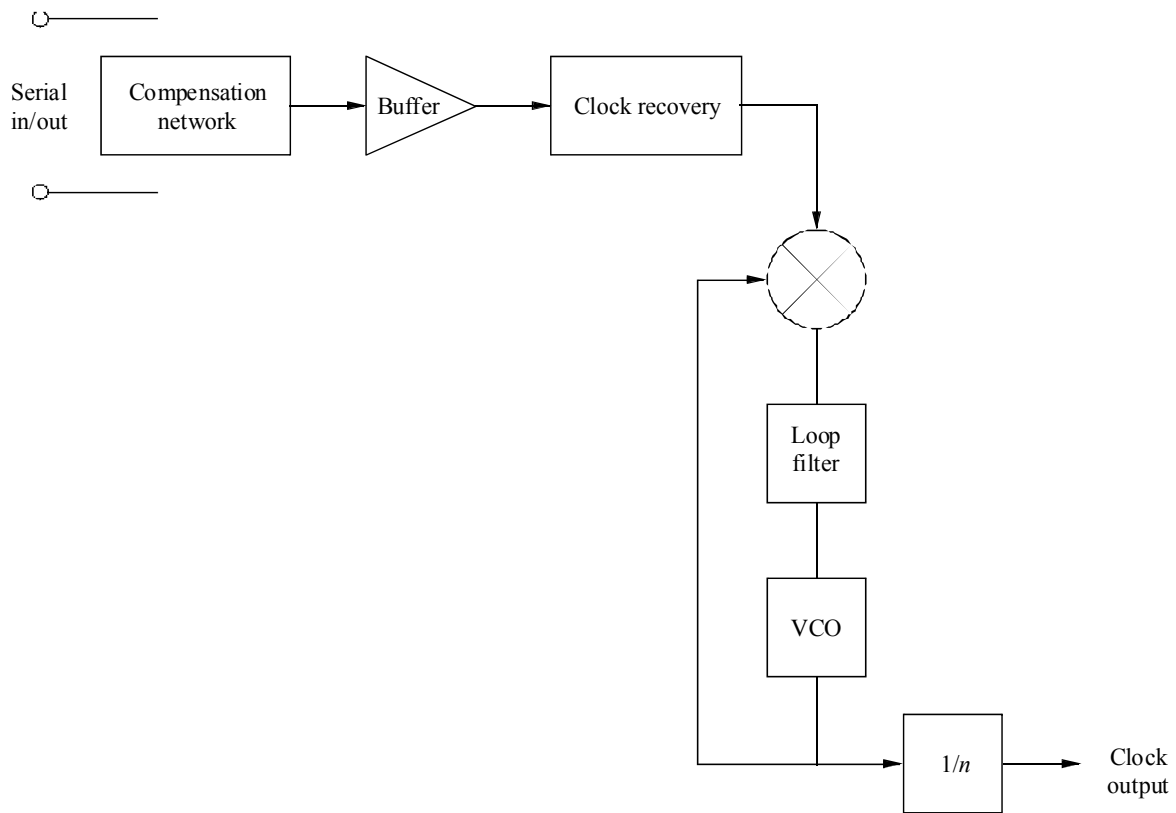
Jitter measurement with oscilloscope and external reference trigger

1363-21

When an external triggering reference is not available, a reference clock must be extracted from the data itself. In this way, greater detail regarding the characteristics of the jitter can be obtained. This can be done by using a clock extractor. A clock extractor is a device that recovers a reference clock from the incoming data stream. The block diagram of a representative clock extractor is shown in Fig. 22. Clock extractors phase lock to the data stream to synthesize a reference clock and this process inherently has a frequency response to it. A clock extractor that has a phase lock loop natural frequency of 1 kHz will only measure jitter frequencies above 1 kHz because the synthesized reference clock extracted from the data will track the frequency variations at rates below 1 kHz. For this reason, clock extractors typically support multiple-loop filter roll-off frequencies.

An enhanced clock extractor, also called a jitter receiver, includes three sections and provides three outputs (see Fig. 23). The first section has a passive loop through input (or power splitter), an equalizer, and a high bandwidth phase locked loop (PLL). The high bandwidth of the PLL results in jitter frequencies below the roll-off of the PLL to be passed along in the extracted output clock (output 1). The upper frequency limit of the jitter reproduced by the clock extractor (f_4 in Fig. 20) is set by the loop bandwidth of this PLL. Additionally, a frequency divider with a settable division ratio is provided prior to the clocking output to permit more time between edge transitions. Because the digital divider will pass along perfectly any input clocking jitter as output jitter, an oscilloscope measurement of jitter amplitudes greater than 1 UI is possible. The second section of the enhanced clock extractor includes a second PLL that incorporates a variable bandwidth loop filter and a high quality (high Q) voltage-controlled crystal oscillator. One setting of loop bandwidth in this second PLL determines the upper bound of the wander frequencies (lower bound of jitter measurements – f_1 in Fig. 20). Another setting of loop bandwidth defines the transition frequency between timing jitter and alignment jitter measurements (f_3 in Fig. 20). The output from this section (output 2) also includes a frequency divider similar to that in the output 1 path for oscilloscope measurement of jitter amplitudes larger than 1 UI.

FIGURE 22
Block diagram of a clock extractor

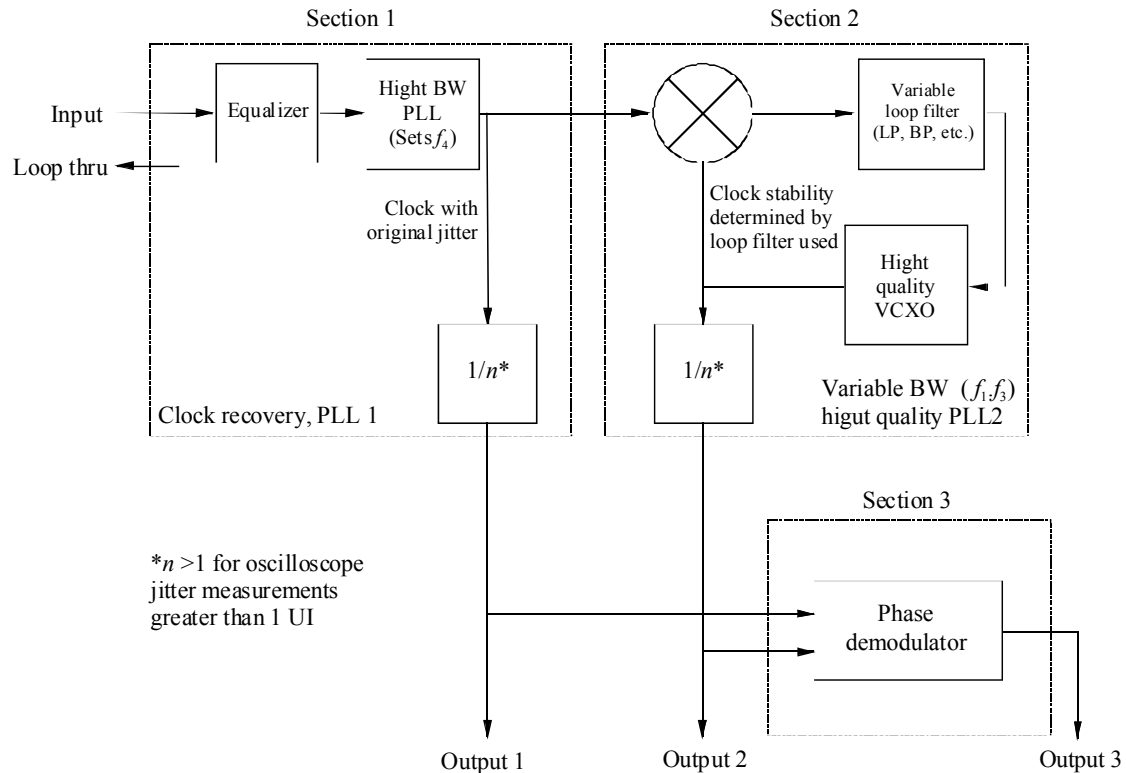


1363-22

The third section of a jitter receiver is a phase demodulator. A phase demodulator creates an analogue voltage that represents the phase difference of two input signals. In this case, the demodulator uses the clocking outputs of the first two sections as inputs. The demodulator output contains the difference in jitter between PLL 2 and PLL 1, which is the input signal jitter between frequencies f_1 (or f_3) and f_4 . This demodulator output (output 3) can then be studied for frequency content. For example, this signal could feed a spectrum analyser, a selective level voltmeter (effectively a tunable receiver), or a filter and voltmeter arrangement to permit measurement of amplitude versus frequency characteristics. This arrangement is well suited for measuring the peak-to-peak jitter over the frequency bands specified for particular pieces of equipment.

FIGURE 23

Jitter receiver block diagram



1363-23

Phase demodulator methods are usually limited in bandwidth to less than 1/10 the clock frequency. Other techniques, such as the eye pattern methods discussed above, may be needed if jitter frequencies above this need investigation. This results from the fact that jitter frequencies as high as 20% of the clock frequency (54 MHz in the case of a 270 Mbit/s system, and occurring at twice the 10-bit word rate) have been known to disrupt proper operation of succeeding devices.

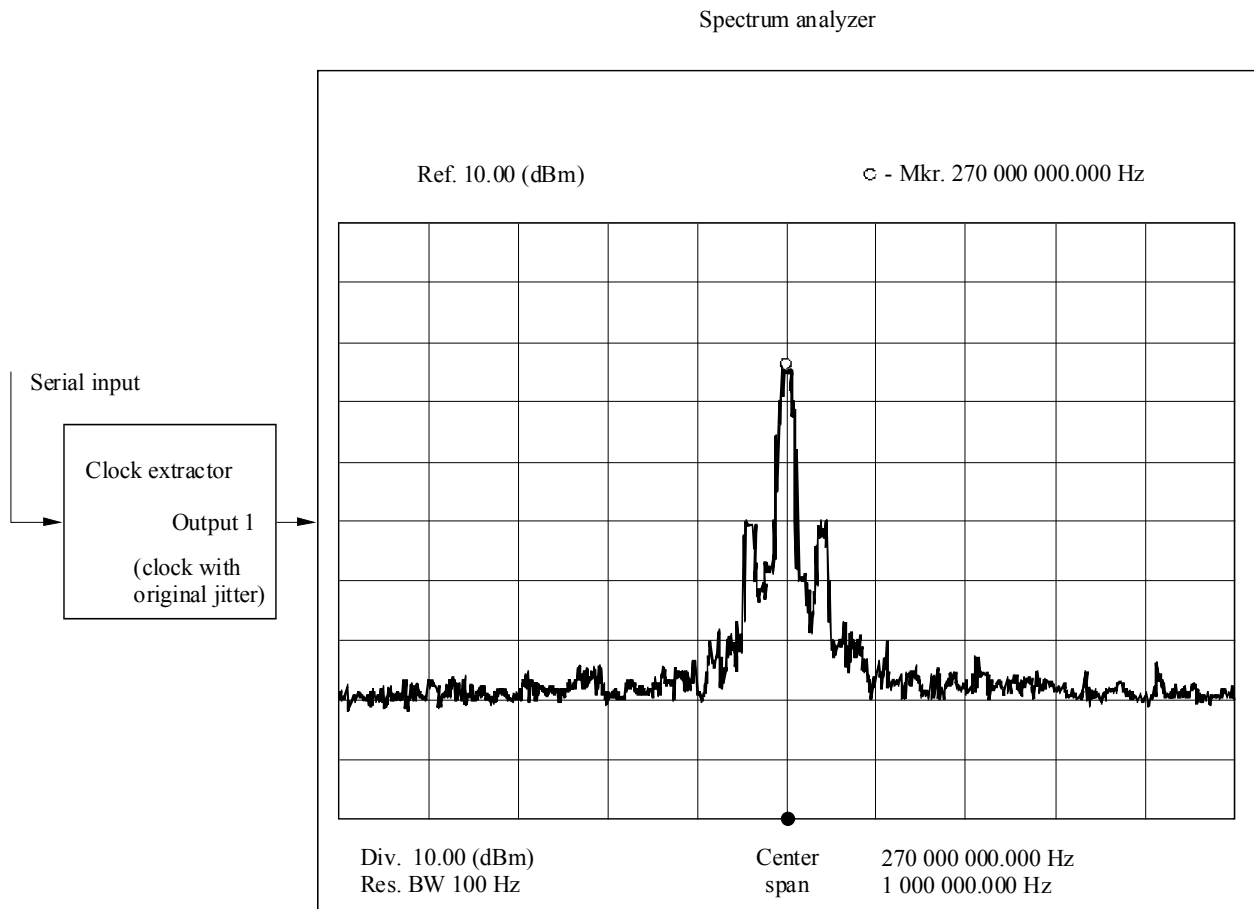
Very useful measurements also result from use of a clock extractor in combination with a spectrum analyser. The exact configuration depends upon the capabilities of the spectrum analyser used.

If a high-frequency spectrum analyser with a narrow resolution bandwidth is available, just the first section of the clock extractor can be used in combination with it to display the spectral characteristics of the jitter in terms of amplitude and frequency. This is shown in Fig. 24, in which the spectrum analyser has been tuned to the clock frequency (270 MHz in this example) and in which two distinct sidebands are visible. These two sidebands represent a single modulating frequency (at about 40 kHz) that has added jitter to the clock somewhere in the system.

If a low-frequency spectrum analyser or an oscilloscope with a built-in FFT (fast Fourier transform) analyser is available, it can be used in conjunction with the complete jitter receiver to create an amplitude versus frequency display similar to that just described. As shown in Fig. 25, just the demodulated sideband energy is displayed. Depending upon the equipment used, this technique is good for measuring jitter up to about half the clock frequency. This limit comes from the bandwidth of the PLL used in the clock extractor of the jitter receiver. This may not be enough, as will be discussed below. Nevertheless, within its bandpass, it is suitable for discovering specific jitter modulation frequencies and their amplitudes.

FIGURE 24

Jitter measurement using a clock extractor and spectrum analyzer



1363-24

The methods described so far are appropriate for oscilloscope jitter measurements in which the jitter is below 1 UI total deviation. If these methods are used to view greater than 1 UI of jitter on an oscilloscope, the result would be an image with the entire eye closed, making it impossible to quantify the jitter. When the jitter exceeds 1 UI and a scope is to be used, the dividers in jitter receiver outputs 1 and 2 can be set to a division ratio higher than 1. This has the effect of reducing the frequency of the carrier by the division ratio used and of reducing the modulation deviation by a proportionate amount. With proper selection of the division ratio, the result is that the phase rotation of the carrier does not exceed 360° , and the eye does not close as it otherwise would at 1 UI. This setup is shown in Fig. 26, wherein output 2 is used for triggering a wideband oscilloscope and output 1 drives the vertical channel. It is important to keep the division ratio as low as possible when making these measurements so as not to mask any word-related jitter effects, as might occur at a ratio of 10 and its submultiples.

5 Equipment specification

The measurement methods available are used for characterizing equipment with respect to jitter performance. They are also used to determine that system implementations do not permit accumulation of jitter sufficient to cause data errors or degraded performance during digital-to-analogue conversion.

FIGURE 25

Jitter measurement using phase demodulator output of jitter receiver

Low frequency spectrum analyzer or scope w/FFT

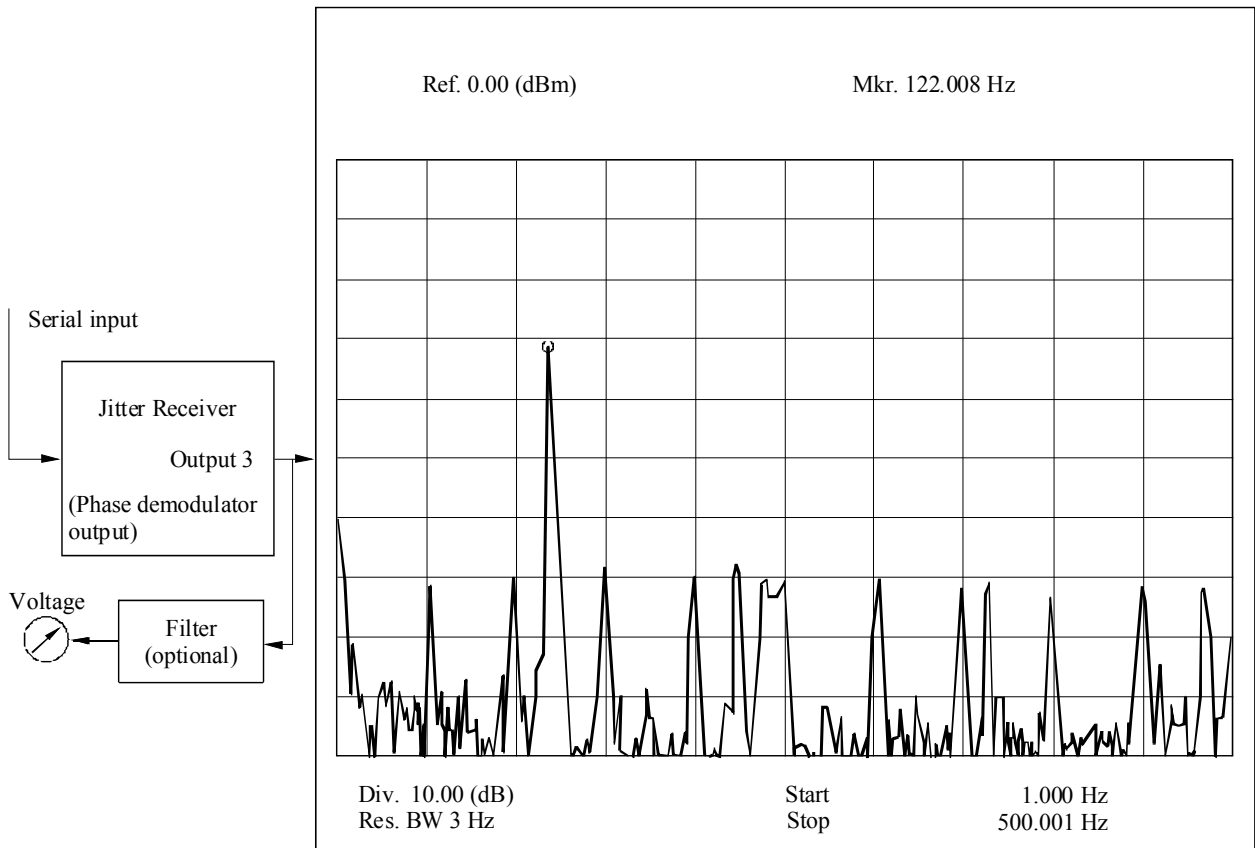
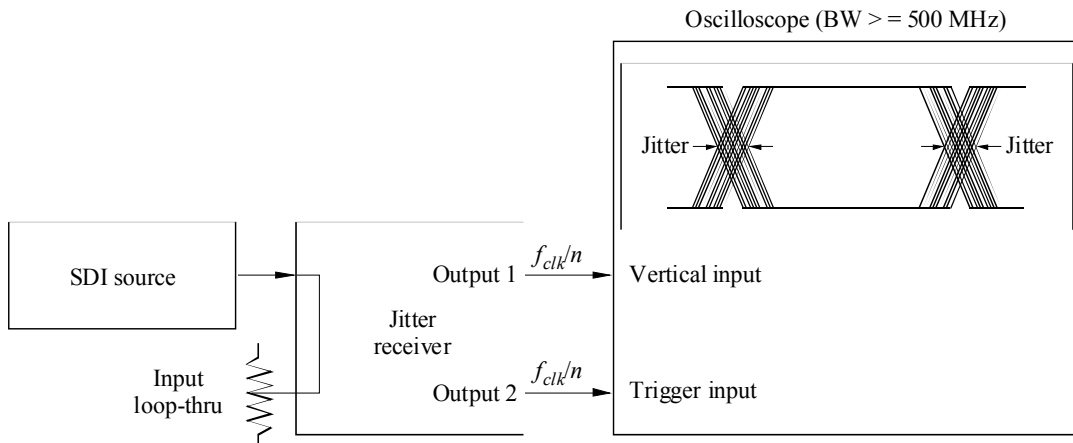


FIGURE 26

Jitter measurement of UI > 1 with oscilloscope and jitter receiver using output frequency division

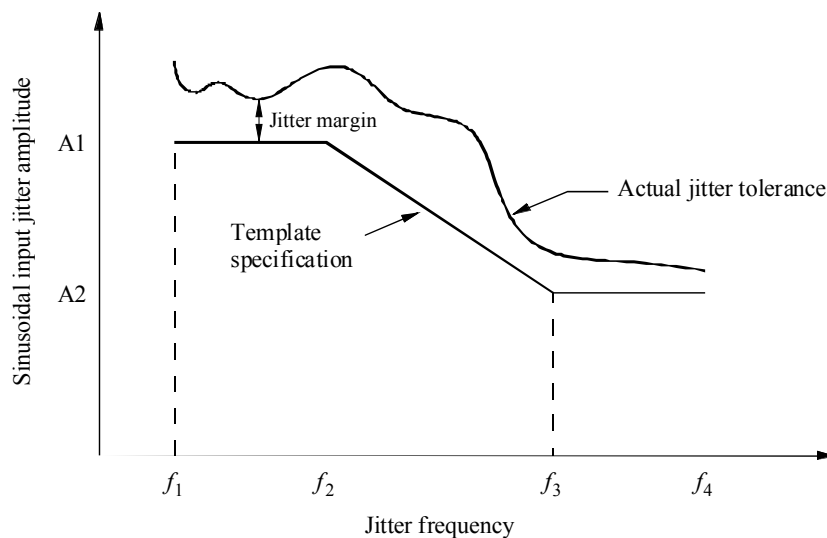


1363-26

The jitter performance of equipment is characterized in several ways. Input jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance. The input jitter tolerance of a piece of equipment can be specified through use of a template, as shown in Fig. 27. The template specifies the minimum input jitter tolerance expected from the equipment. The actual input jitter tolerance measured (also shown in Fig. 27) will be higher than the template for properly operating units.

FIGURE 27

Input jitter tolerance template and a compliant input jitter tolerance

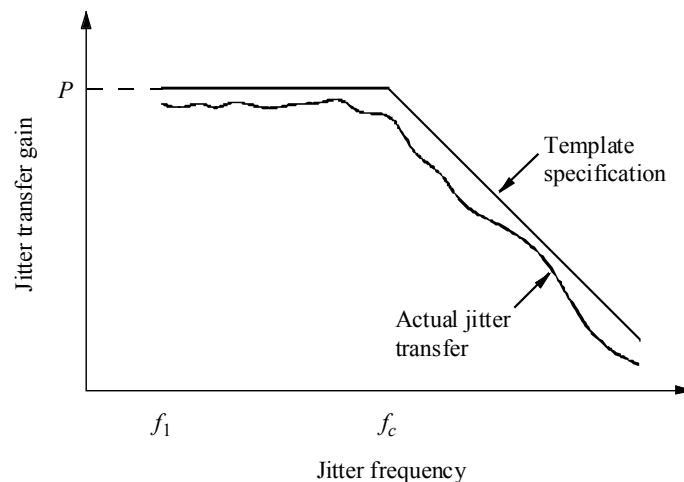


1363-27

Jitter transfer is jitter that occurs on the output of equipment resulting from jitter applied to the input of that equipment. The jitter transfer function is the ratio of the output jitter to the applied input jitter as a function of frequency. A template is used to specify the jitter transfer function in terms of jitter gain versus frequency. This is shown in Fig. 28, where a compliant jitter transfer function is shown as falling below the template specification. The template is specified and measurements are made from f_1 (the low-frequency specification limit) to f_c (the upper band edge of the jitter transfer bandpass).

FIGURE 28

Jitter transfer template and a compliant jitter transfer function



1363-28

Jitter at equipment outputs is broken into two categories. Intrinsic jitter is the amount of jitter at the equipment output when the input to the equipment is jitter-free. It is essentially the jitter that is generated by the equipment. Output jitter is the amount of jitter measured at the equipment output when the equipment is embedded in a system. It comprises the sum of the jitter transfer of the jitter appearing at the equipment input and the intrinsic jitter of the equipment.

6 System considerations

Jitter usually accumulates as signals pass through a system. Error-free operation requires that the output jitter at one piece of equipment does not exceed the input jitter tolerance of the succeeding equipment item. Jitter specifications allow estimating the jitter accumulation in a cascade of digital equipment.

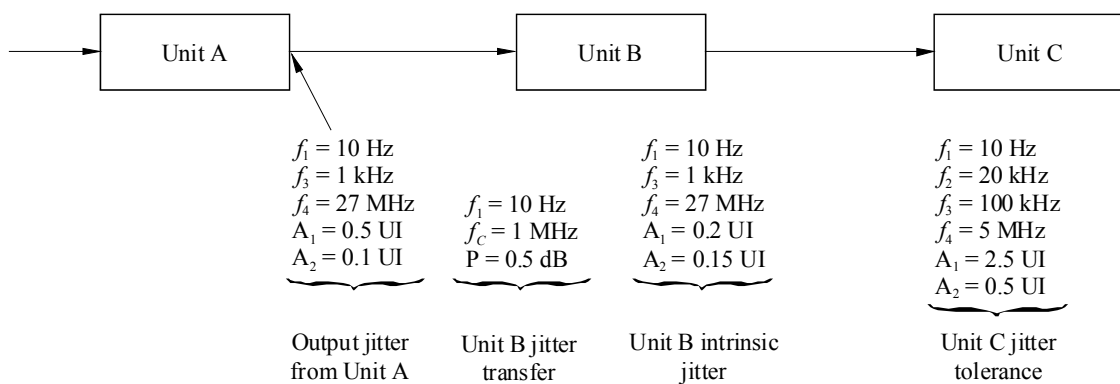
Models for jitter accumulation separate jitter into two categories: random and systematic. Random jitter is defined as jitter that is uncorrelated with other jitter generated in the system. Edge jitter caused by thermal noise in a slicing circuit is an example of random jitter. Since it is uncorrelated, random jitter adds on a power basis: the amplitude increases root-sum-square. Systematic jitter is jitter that is completely correlated with other jitter in the system. Timing variations caused by specific data sequences are an example of systematic jitter, since in a cascade of identical regenerators the same behaviour occurs at each one. Since it is correlated, systematic jitter accumulates arithmetically.

Most jitter is a combination of random and systematic. After passing through several regenerators, however, systematic jitter usually dominates because of the arithmetic accumulation. Accordingly, simple accumulation models treat all jitter as systematic.

Jitter accumulation is estimated as follows:

1. Jitter at an equipment input is multiplied by the equipment's jitter transfer function.
2. This scaled jitter is added to the equipment's intrinsic jitter to get output jitter.
3. This output jitter becomes the input jitter for the next stage, and the process repeated.
4. At no point can the output jitter exceed the input jitter tolerance of the next stage.

EXAMPLE:



1363-28b

Step 1: Multiply output jitter from unit A by unit B's jitter transfer function

Unit B's jitter transfer function shows 0.5 dB peaking over 10 Hz to 1 MHz, rolling off beyond 1 MHz. 0.5 dB corresponds to a gain of 1.06.

$$f_1 \text{ to } f_c \text{ (10 Hz to 1 MHz): } (A_1) \log^{-1} (P/20) = (0.5 \text{ UI}) (1.06) = 0.53 \text{ UI}$$

$$f_3 \text{ to } f_c \text{ (1 kHz to 1 MHz): } (A_2) \log^{-1} (P/20) = (0.1 \text{ UI}) (1.06) = 0.11 \text{ UI}$$

Note that the jitter calculation was limited to 1 MHz (f_c), even though the input jitter (output jitter from unit A) was specified to 27 MHz (f_4). This is because unit B's jitter transfer function low pass filters the input jitter to 1 MHz. Even if higher frequency terms are present, they are not propagated by unit B and hence do not figure into the accumulation calculation.

Step 2: Add unit B intrinsic jitter to jitter transferred by unit B to get unit B output jitter

Above f_1 (10 Hz): Output jitter = 0.53 UI + 0.2 UI = 0.73 UI

Above f_3 (1 kHz): Output jitter = 0.11 UI + 0.15 UI = 0.26 UI

Above f_c (1 MHz): Output jitter = 0.15 UI

The third entry results because there is no jitter transfer above f_c (1 MHz). Thus, the only output jitter above this frequency is unit B's intrinsic jitter. Although it is unknown if the 0.15 UI occurs

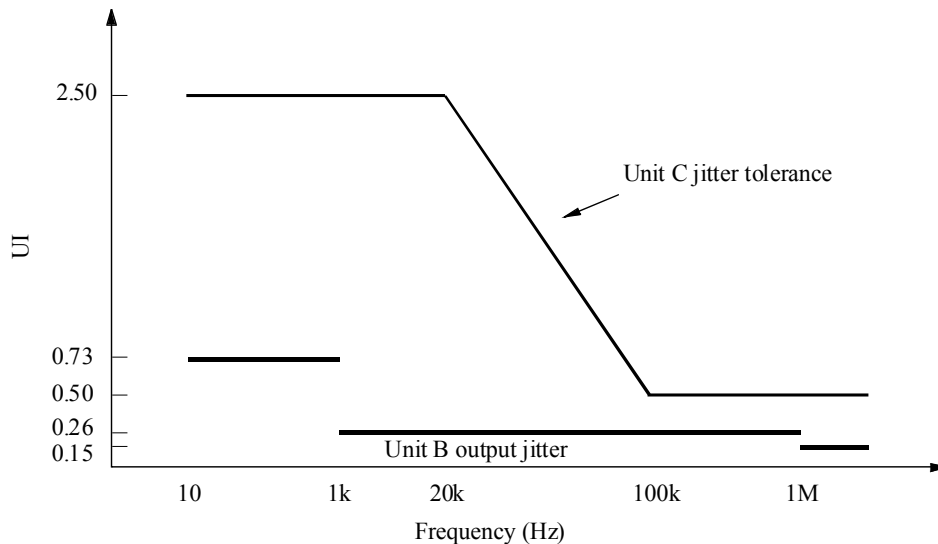
between 1 kHz and 1 MHz, or above 1 MHz, the practice is to assume a constant magnitude over the entire f_3 to f_4 range.

Step 3: Compare unit B output jitter with unit C input jitter tolerance

Unit C jitter tolerance requires that jitter above f_3 (100 kHz) must be less than 0.5 UI, and jitter between f_1 (10 Hz) and f_2 (20 kHz) must be less than 2.5 UI. Unit B output jitter is 0.15 UI above f_c (1 MHz), 0.26 UI above f_3 (1 kHz), and 0.73 UI above f_1 (10 Hz). A pessimistic but convenient assumption is that all 0.73 UI occurs between f_1 and f_3 (10 Hz and 1 kHz). Note that unit B's output jitter is less than unit C's input jitter tolerance (see Fig. 29).

Thus, this cascade of equipment would work.

FIGURE 29
Unit B output jitter compared with unit C jitter tolerance



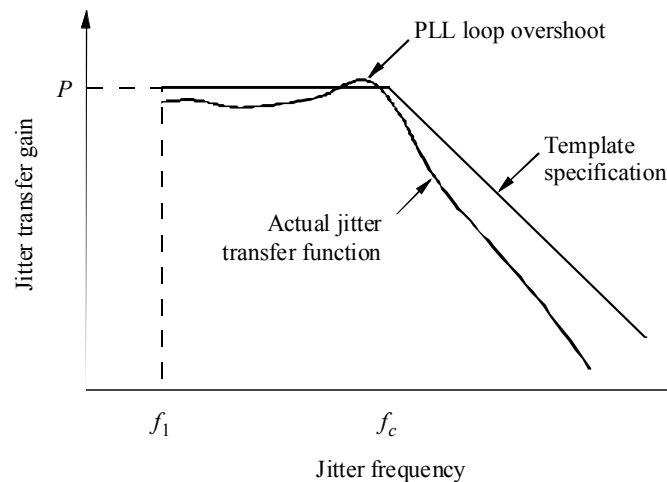
1363-29

The simple method described above allows paper calculations of a proposed cascade of equipment. This requires obtaining jitter tolerance, jitter transfer, and intrinsic jitter specifications from the equipment manufacturer. If unavailable, these parameters can be measured.

Jitter failures result when output jitter exceeds the following equipment's input jitter tolerance. Common causes of this in a system are:

1. Excessive intrinsic jitter, normally the result of poor equipment design or equipment failure.
2. After a cascade of equipment having jitter transfer up to f_c , adding a device whose jitter tolerance breakpoint f_3 is much lower than frequency f_c . Jitter will accumulate arithmetically below f_c , and will eventually exceed the high-frequency jitter tolerance A_2 . There is essentially no jitter accumulation above f_c .
3. Peaking in the jitter transfer function, usually near f_c (see Fig. 30). A cascade of equipment with this characteristic can show pronounced jitter growth.

FIGURE 30
Jitter transfer function showing jitter peaking



1363-30

Items 2 and 3 are good examples of why published specifications on jitter transfer and jitter tolerance are important. Item 2 can be avoided by suitable equipment choice, by suitably ordering a cascade of equipment, or by installing a jitter remover prior to the device with the low f_3 jitter tolerance breakpoint. Item 3 can be avoided with suitable equipment choice (small jitter peaking), or designed around jitter removers, or by limiting the length of the cascade. All of these solutions require knowing the jitter transfer and tolerance of components in the system.

7 Mitigating jitter

It may be necessary to eliminate jitter at various points in a system. This could be for reasons of jitter accumulation sufficient to exceed the input jitter tolerance of a succeeding device, as just discussed, or it could be to permit a high-quality conversion to analogue form. Jitter causes non-linearity in digital-to-analogue (D/A) converters. High quality D/A conversion, therefore, requires removal of any jitter accompanying a signal if the conversion clock is derived from the signal.

A jitter remover works by converting serial digital signals back to parallel form, passing them through a first-in-first-out (FIFO) register, and then re-serializing them using a highly stable clock. Usually this highly stable clock is referenced to a synchronization signal like black burst. As shown in Fig. 31, the input to the jitter remover is structured very much like the input to any equipment with an SDI input. This is followed by a relatively small FIFO with sufficient length to accommodate the longest time variations caused by the highest jitter amplitudes expected to be encountered. Finally, the high quality clock source drives either a serializer or a D/A converter to provide a virtually jitter-free output. Devices of this sort can be applied in a system as often as necessary to control jitter accumulation or to ensure linear analogue outputs. Care must be taken in implementing jitter removers to account for the additional delay they cause and to ensure that the delay is predictable.

FIGURE 31
Block diagram of "jitter remover"

