RECOMMENDATION ITU-R BT.1120-1

DIGITAL INTERFACES FOR 1125/60/2:1 AND 1250/50/2:1 HDTV STUDIO SIGNALS

(Question ITU-R 65/11)

(1994-1998)

The ITU Radiocommunication Assembly,

considering

a) that in the scope of Recommendation ITU-R BT.709 studio standards for HDTV have been developed;

b) that Recommendation ITU-R BT.1200 specifies a flexible system description based on the carriage of declarable parameter values;

c) that there exist signal specifications for HDTV studio systems based on 1125 lines, 60 Hz field rate, 2:1 interlace and 1250 lines, 50 Hz field rate, 2:1 interlace, based on the above Recommendations;

d) that a whole range of equipment based on the above systems has been developed and is commercially available, including all those necessary for broadcasting chains and for industrial applications;

e) that many programmes are being produced in both systems using the above equipments and that in the development of broadcasting and other services there is an increasing need for HDTV production installations;

f) that the use of digital technology and digital interconnection is highly desirable to reach and maintain the level of performance required for HDTV;

g) that there are clear advantages for establishing interface specifications for HDTV production installations,

recommends

that the specifications described in this Recommendation should be used as the basic digital coding as well as the bit-parallel and bit-serial interfaces for the 1125/60 and 1250/50 studio signals.

1 Digital representation

1.1 Coding characteristics

The signals to be digitized should comply with the characteristics described in Recommendation ITU-R BT.709.

1.2 Construction of digital signals

Digital representation of R, G, B, Y, C_R and C_B may be obtained using the following relationship. Further study is required in terms of conversion between the data obtained with 8- and 10-bit quantization.

$$
\begin{aligned}
R_d &= [\ \mathrm{Int}\ \{\ (219 \times D) \times E'_R + (16 \times D) + 0.5\ ] / D \\
G_d &= [\ \mathrm{Int}\ \{\ (219 \times D) \times E'_G + (16 \times D) + 0.5\ ] / D \\
B_d &= [\ \mathrm{Int}\ \{\ (219 \times D) \times E'_B + (16 \times D) + 0.5\ ] / D \\
Y_d &= [\ \mathrm{Int}\ \{\ (219 \times D) \times E'_Y + (16 \times D) + 0.5\ ] / D \\
C_{Rd} &= [\ \mathrm{Int}\ \{\ (224 \times D) \times E'_{CR} + (128 \times D) + 0.5\ ] / D \\
C_{Bd} &= [\ \mathrm{Int}\ \{\ (224 \times D) \times E'_{CB} + (128 \times D) + 0.5\ ] / D
\end{aligned}
$$

where D takes either the value 1 or 4, corresponding to 8-bit or 10-bit quantization respectively; E'_G, E'_B, E'_R and E'_Y denote analogue R, G, B and luminance signals that have been normalized to span the range 0.0 to 1.0, while E'_{CR} and E'_{CB} denote analogue colour-difference signals that have been normalized to span the range –0.5 to +0.5.

TABLE 1

Digital coding parameters

Item	Parameter	Value			
		1125/60		1250/50	
1	Coded signals Y, C_R, C_B or R, G, B	These signals are obtained from gamma pre-corrected signals, namely E'_Y, $E'_R - E'_Y$, $E'_B - E'_Y$ or E'_R, E'_G, E'_B (1)			
2	Sampling lattice – R, G, B, Y	Orthogonal, line and picture repetitive			
3	Sampling lattice signal – C_R, C_B	Orthogonal, line and picture repetitive, co-sited with each other and with alternate Y samples. The first active colour-difference samples are co-sited with the first active Y sample			
4	Number of active lines	1035	1080	1152	
5	Sampling frequency (2) – R, G, B, Y	74.25 MHz $\pm 10 \times 10^{-6}$	74.25 MHz or 74.25/ 1.001 MHz $\pm 10 \times 10^{-6}$	72 MHz $\pm 0.1 \times 10^{-6}$	54 MHz $\pm 0.1 \times 10^{-6}$
6	Sampling frequency (2) – C_R, C_B	Half of luminance sampling frequency			
7	Number of samples/line – R, G, B, Y – C_R, C_B	2200 1100		2304 1152	1728 864
8	Number of active samples/line – R, G, B, Y – C_R, C_B	1920 960			1440 720
9	Position of the first active Y, C_R, C_B sampling instants with respect to the analogue sync timing reference O_H (6) (see Fig. 5)	192 T		256 T	192 T
10	Coding format	Uniformly quantized PCM for each of the video component signals			
		8 or 10 bit/sample		8 or 10 bit/sample 10 bit preferable	
11	Quantization level assignment (3) – Video data – Timing references	1.00 through 254.75 0.00 and 255.75			
12	Quantization levels (4) – Black level R, G, B, Y – Achromatic level C_R, C_B – Nominal peak R, G, B, Y C_R, C_B	16.00 128.00 235.00 16.00 and 240.00			
13	Filter characteristics (5) – R, G, B, Y – C_R, C_B	See Fig. 1 See Fig. 2		See Fig. 3 See Fig. 4	

(1) The values for $E'_R - E'_Y$ and $E'_B - E'_Y$ are assumed to be re-normalized.

(2) The sampling clock must be locked to the line frequency.

(3) To reduce confusion when using 8-bit and 10-bit systems together, the two LSBs of the 10-bit system are read as two fractional bits. The quantization scale in an 8-bit system reaches from 0 to 255 in steps of 1, and in a 10-bit system from 0.00 to 255.75 in steps of 0.25.

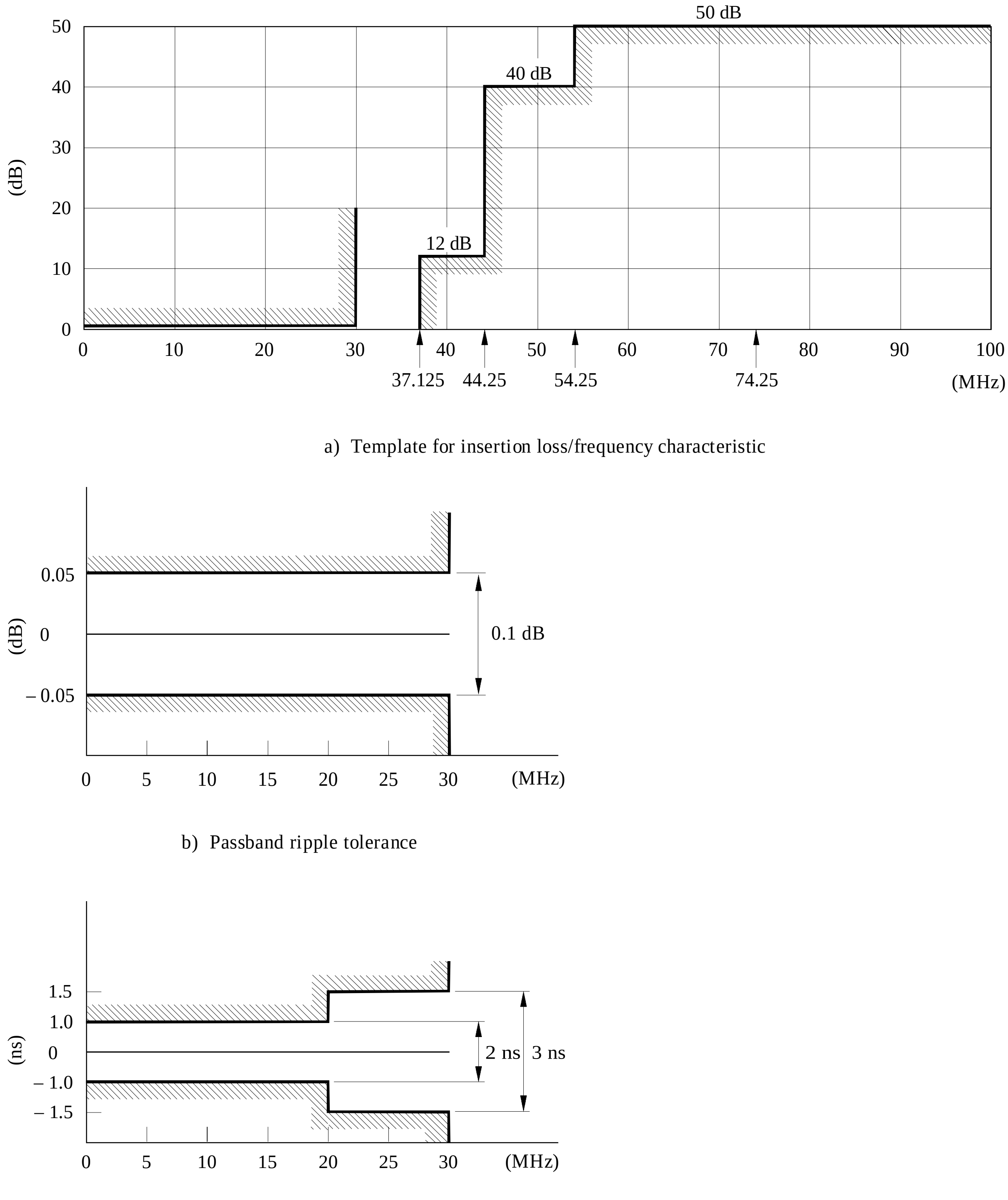
(4) These levels refer to precise nominal video levels. Signal processing may occasionally cause the signal level to deviate outside these ranges.

(5) For 1125/60, the characteristics are specified as a design guideline. For 1250/50, the templates specified facilitate the implementation of practical filters.

(6) T denotes the clock period: for 1125/60, 13.468 ns when the sampling frequency is 74.25 MHz and 13.481 ns when the sampling frequency is 74.25/1.001 MHz. For 1250/50, values are 13.889 ns when the sampling frequency is 72 MHz and 18.519 ns when the sampling frequency is 54 MHz.

FIGURE 1

Specification for a luminance or RGB signal filter for 1125/60



a) Template for insertion loss/frequency characteristic

b) Passband ripple tolerance

c) Passband group-delay tolerance

Note 1 – Ripple and group delay are specified relative to their values at 100 kHz.

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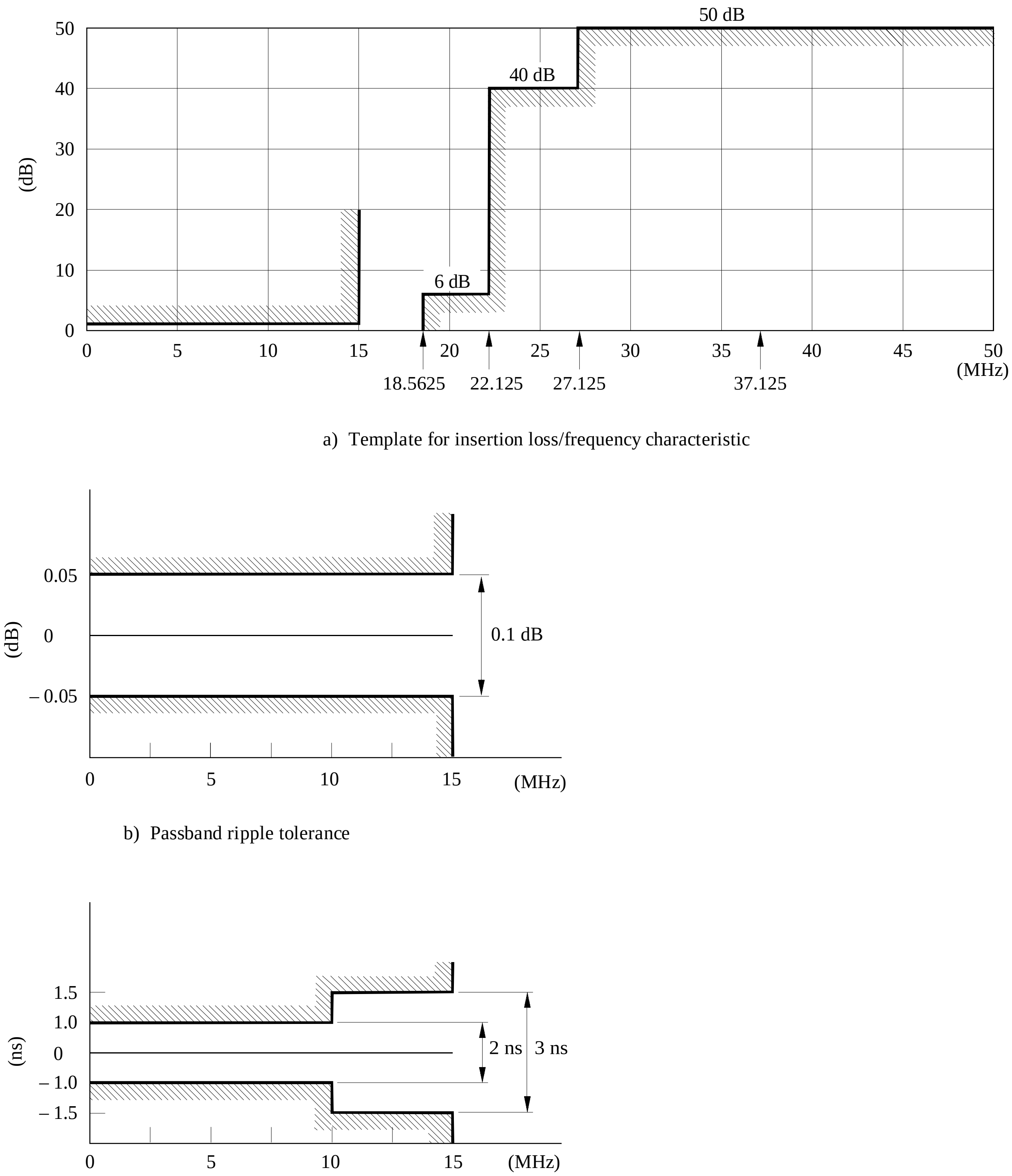
FIGURE 2

Specification for a colour-difference signal filter for 1125/60



a) Template for insertion loss/frequency characteristic

b) Passband ripple tolerance

c) Passband group-delay tolerance

Note 1 – Ripple and group delay are specified relative to their values at 100 kHz.

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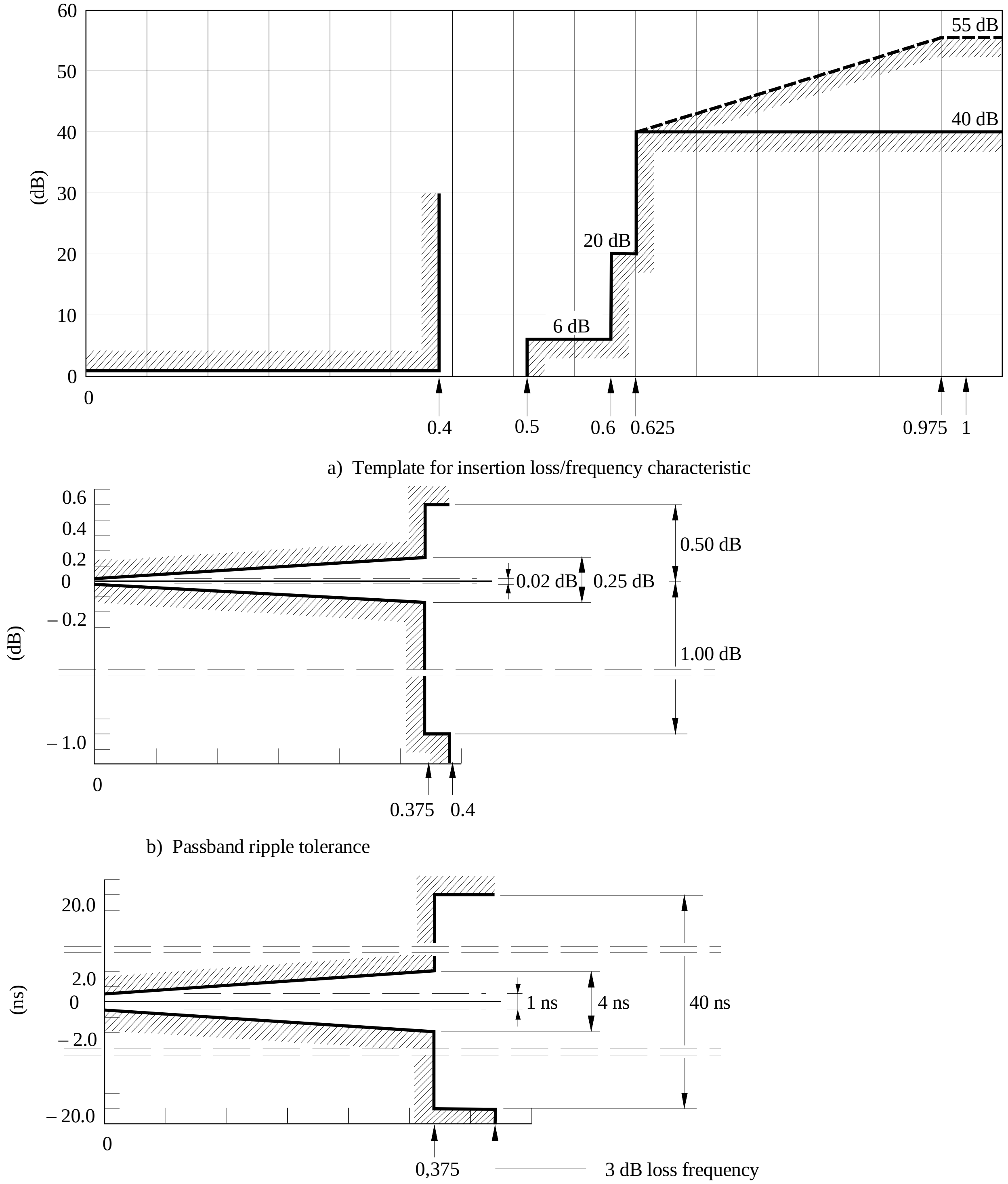
FIGURE 3

Specification for a luminance or RGB signal filter for 1250/50



c) Passband group-delay tolerance

Note 1 – Figures on the horizontal scale are given in values relative to the sampling frequency fs (see item 5, Table 1).

Note 2 – In a digital implementation for sample rate conversion:

– the insertion loss should be at least 55 dB above 0.975 fs (dashed-line template);

– the amplitude/frequency characteristic (on linear scale) should be skew symmetric about the half amplitude point;

– the group delay distortion should be zero by design.

Note 3 – Ripple and group delay are specified relative to their values at 5 kHz.

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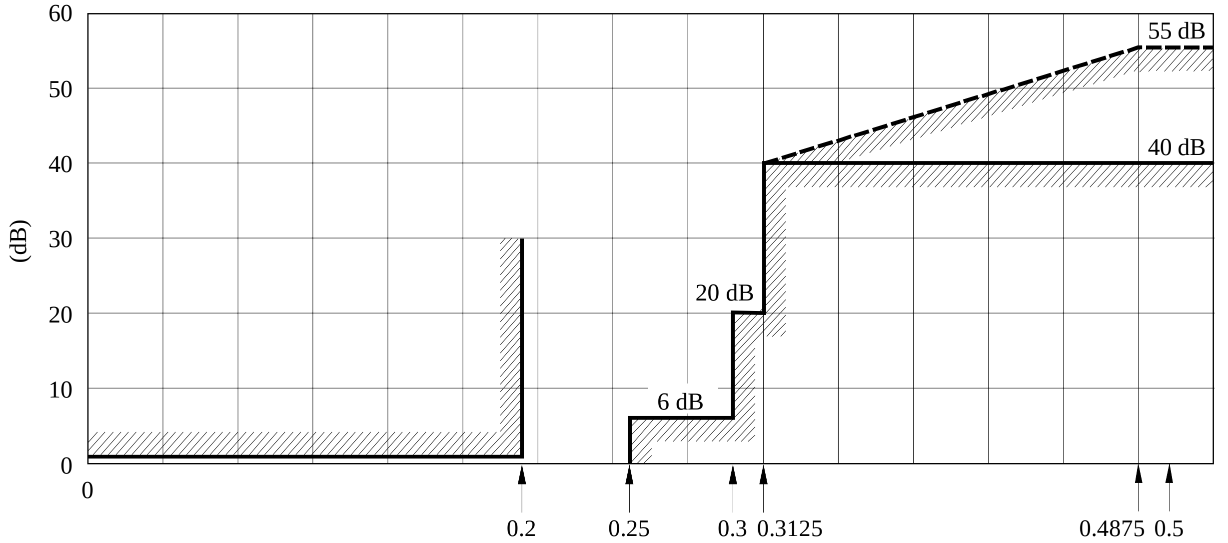
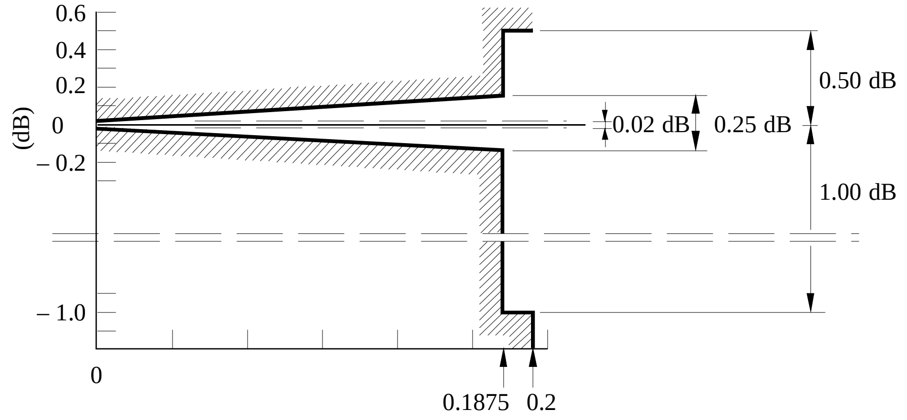
FIGURE 4

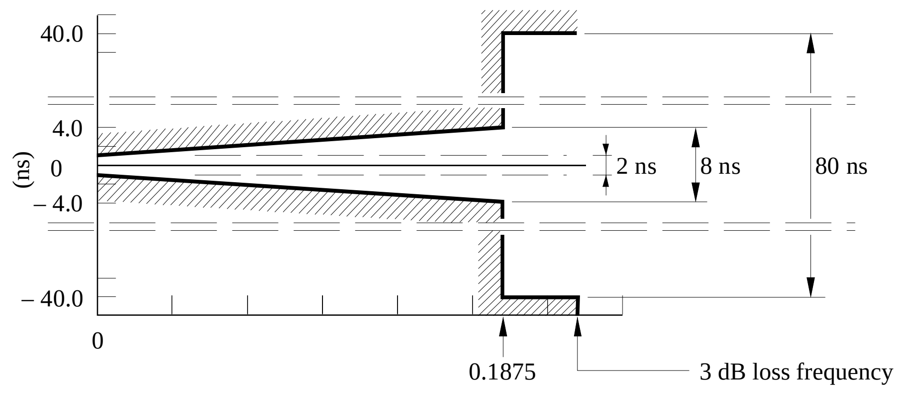
Specification for a colour-difference signal filter for 1250/50



a) Template for insertion loss/frequency characteristic



b) Passband ripple tolerance



c) Passband group delay tolerance

Note 1 – Figures on the horizontal scale are given in values relative to the luminance sampling frequency fs (see item 5, Table 1).

Note 2 – In a digital implementation for sample rate conversion:

– the insertion loss should be at least 55 dB above 0.4875 fs (dashed-line template);
– the amplitude/frequency characteristic (on linear scale) should be skew symmetric about the half amplitude point;
– the group delay distortion should be zero by design.

Note 3 – Ripple and group delay are specified relative to their values at 5 kHz.

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2 Digital interface

The interface provides a unidirectional interconnection between a single source and a single destination. The data signals are in the form of binary information and are coded accordingly:

– video data (8-bit or 10-bit words for 1125/60 and 1250/50);

– timing reference and identification codes (8-bit or 10-bit words for 1125/60, 10-bit words only for 1250/50);

– ancillary data.

2.1 Video data

Y, C_R, C_B signals are handled as 20-bit words by time-multiplexing C_R and C_B components. Each 20-bit word corresponds to a colour-difference sample and a luminance sample. The multiplex is organized as:

$$(C_{B1}\ Y_1)\ (C_{R1}\ Y_2)\ (C_{B3}\ Y_3)\ (C_{R3}\ Y_4)\ ...$$

where Y_i indicates the i-th active sample of a line, while C_{Bi} and C_{Ri} indicate the colour-difference samples of C_R and C_B components co-sited with the Y_i sample. Note that the index "i" on colour-difference samples takes only odd values due to the half-rate sampling of the colour-difference signals.

The data words corresponding to digital levels 0.00 through 0.75 and 255.00 through 255.75 are reserved for data identification purposes and must not appear as video data.

For 1125/60, R, G and B signals are handled as 30-bit words in addition to the above 20-bit words for Y, C_R and C_B signals.

2.2 Video timing relationship with analogue waveform

For 1125/60, the digital line occupies 2200 clock periods. It begins at 88 clock periods prior to the reference transition (O_H) of the analogue synchronizing signal in the corresponding line. The digital active line begins at 192 clock periods after the reference transition (O_H).

For 1250/50 at 72 MHz sampling frequency, the digital line occupies 2304 clock periods. It begins at 128 clock periods prior to the reference transition (O_H) of the analogue synchronizing signal in the corresponding line. The digital active line begins at 256 clock periods after the reference transition (O_H).

For 1250/50 at 54 MHz sampling rate, the digital line occupies 1728 clock periods. It begins at 96 clock periods prior to the reference transition (O_H) of the analogue synchronizing signal in the corresponding line. The digital active line begins at 192 clock periods after the reference transition (O_H).

See Fig. 5 and Table 2 for detailed timing relationship in the line interval.

The start of digital field is fixed by the position specified for the start of the digital line. See Fig. 6 and Table 3 for detailed relationship in field interval.

2.3 Video timing reference codes (SAV and EAV)

There are two timing reference codes, one at the beginning of each video data block (start of active video; SAV) and the other at the end of each video data block (end of active video; EAV). These codes are contiguous with the video data, and continue during the field blanking interval, as shown in Fig. 6.

Each code consists of a four-word sequence. The bit assignment of the word is given in Table 4. The first three words are fixed preamble and the fourth word carries the information that defines field identification (F), field blanking period (V), and line blanking period (H). In a 1125/60 8 bit implementation bits Nos. 9 to 2 inclusive are used; note in 1250/50 all 10 bits are required.

The bits F and V change state synchronously with EAV at the beginning of the digital line.

FIGURE 5

Data format and timing relationship to analogue waveform

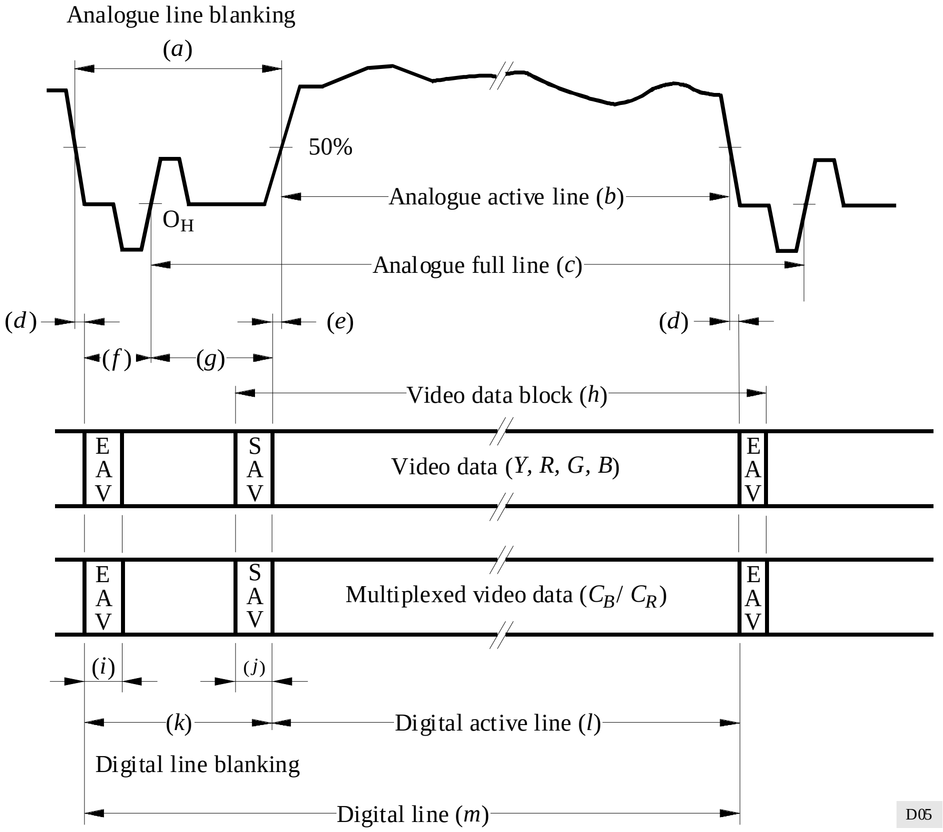


TABLE 2

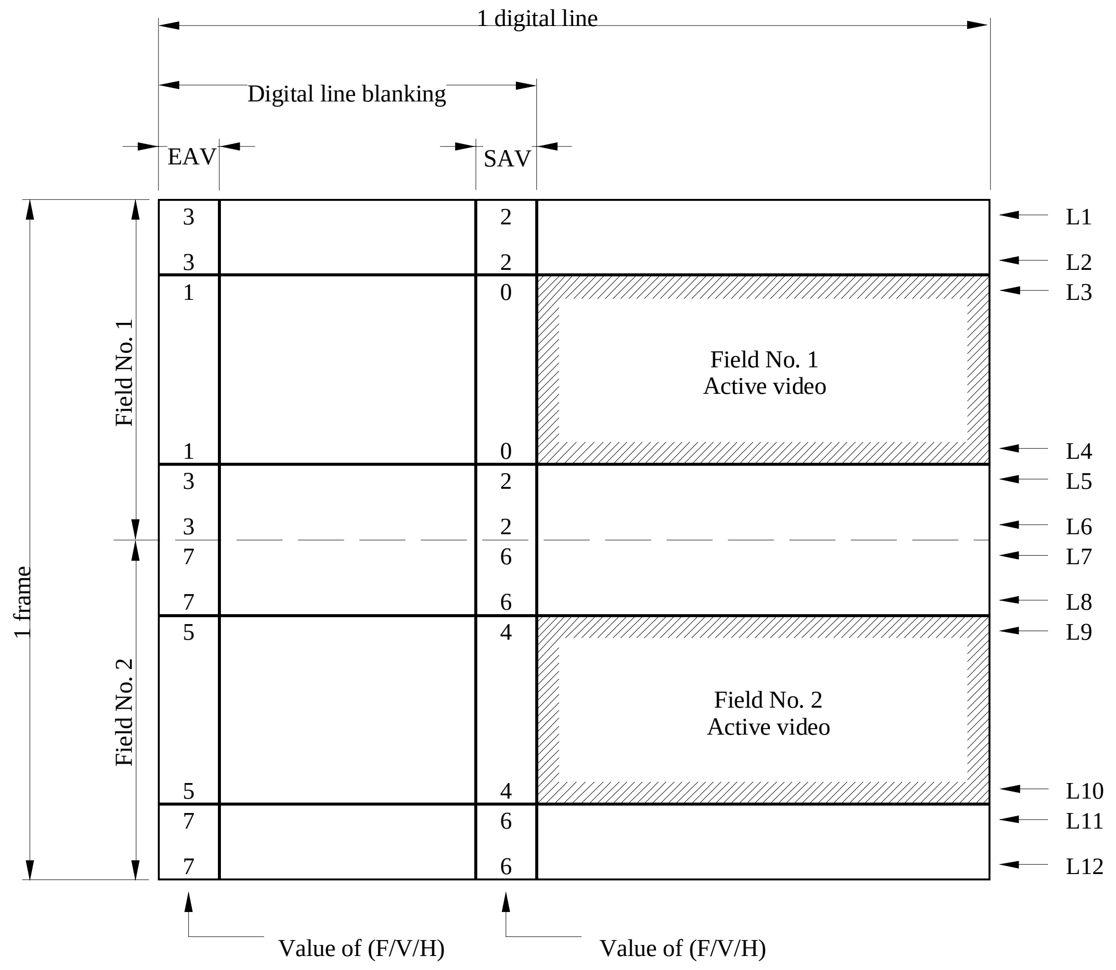
Line interval timing specifications

Symbol	Parameter	Value		
		1125/60	1250/50	
	Number of active Y samples per line	1920	1920	1440
a	Analogue line blanking	3.771 µs nominal	6.00 µs nominal	
b	Analogue active line	25.859 µs nominal	26.00 µs nominal	
c	Analogue full line	29.630 µs nominal	32.00 µs nominal	
d	Duration between end of analogue active video and start of EAV	0-6 *T*	24 *T*	18 *T*
e	Duration between end of SAV and start of analogue active video	0-6 *T*	24 *T*	18 *T*
f	Duration between start of EAV and analogue timing reference O_H	88 *T*	128 *T*	96 *T*
g	Duration between analogue timing reference O_H and end of SAV	192 *T*	256 *T*	192 *T*
h	Video data block	1928 *T*		1478 *T*
i	Duration of EAV	4 *T*		
j	Duration of SAV	4 *T*		
k	Digital line blanking	280 *T*	384 *T*	288 *T*
l	Digital active line	1920 *T*		1440 *T*
m	Digital line	2200 *T*	2304 *T*	1728 *T*

NOTE 1 – T denotes the clock period: for 1125/60, 13.468 ns when the sampling frequency is 74.25 MHz and 13.481 ns when the sampling frequency is 74.25/1.001 MHz. For 1250/50, values are 13.889 ns when the sampling frequency is 72 MHz and 18.519 ns when the sampling frequency is 54 MHz.

FIGURE 6

Field timing relationship



Note 1 – The values of (F/V/H) for EAV and SAV represent the status of bits for F, V, and H, in a way that the three-bit word composed of F, V, H represents a binary number expressed in decimal notation (F corresponding to MSB and H to LSB). For example, the value 3 represents the bits of F = 0, V = 1 and H = 1.

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TABLE 3

Field interval timing specifications

Symbol	Definition	Digital line number		
		1125/60		1250/50
	Number of active lines	1035	1080	1152
L1	First line of field No. 1	1		
L2	Last line of digital field blanking No. 1	40	20	44
L3	First line of field No. 1 active video	41	21	45
L4	Last line of field No. 1 active video	557	560	620
L5	First line of digital field blanking No. 2	558	561	621
L6	Last line of field No. 1	563		625
L7	First line of field No. 2	564		626
L8	Last line of digital field blanking No. 2	602	583	669
L9	First line of field No. 2 active video	603	584	670
L10	Last line of field No. 2 active video	1120	1123	1245
L11	First line of digital field blanking No. 1	1121	1124	1246
L12	Last line of field No. 2	1125		1250

NOTE 1 – Digital field blanking No. 1 denotes the field blanking period that is prior to the active video of field No. 1, and digital field blanking No. 2 denotes that prior to the active video of field No. 2.

TABLE 4

Bit assignment for video timing reference codes

Word	Bit number									
	9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
First	1	1	1	1	1	1	1	1	1	1
Second	0	0	0	0	0	0	0	0	0	0
Third	0	0	0	0	0	0	0	0	0	0
Fourth	1	F	V	H	P_3	P_2	P_1	P_0	0	0

F = 1 during field No. 2
= 0 during field No. 1

V = 1 during field blanking
= 0 elsewhere

H = 1 in EAV
= 0 in SAV

NOTE 1 – P_0, P_1, P_2, P_3 in the fourth word are the protection bits (see Table 5).

The value of protection bits, P_0 to P_3, depends on the F, V, and H as shown in Table 5. The arrangement permits one-bit errors to be corrected and two-bit errors to be detected at the receiver, but only in the 8 most-significant bits, as shown in Table 6.

TABLE 5

Protection bits for SAV and EAV

	SAV/EAV bit status			Protection bits					
Bit 9 (fixed)	8 (F)	7 (V)	6 (H)	5 (P_3)	4 (P_2)	3 (P_1)	2 (P_0)	1 (fixed)	0 (fixed)
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	0	0
1	0	1	0	1	0	1	1	0	0
1	0	1	1	0	1	1	0	0	0
1	1	0	0	0	1	1	1	0	0
1	1	0	1	1	0	1	0	0	0
1	1	1	0	1	1	0	0	0	0
1	1	1	1	0	0	0	1	0	0

TABLE 6

Error corrections using protection bits (P_3-P_0)

Received bits 5-2	Received bits 8-6 for F, V and H							
for P_3-P_0	000	001	010	011	100	101	110	111
0000	000	000	000	–	000	–	–	111
0001	000	–	–	111	–	111	111	111
0010	000	–	–	011	–	101	–	–
0011	–	–	010	–	100	–	–	111
0100	000	–	–	011	–	–	110	–
0101	–	001	–	–	100	–	–	111
0110	–	011	011	011	100	–	–	011
0111	100	–	–	011	100	100	100	–
1000	000	–	–	–	–	101	110	–
1001	–	001	010	–	–	–	–	111
1010	–	101	010	–	101	101	–	101
1011	010	–	010	010	–	101	010	–
1100	–	001	110	–	110	–	110	110
1101	001	001	–	001	–	001	110	–
1110	–	–	–	011	–	101	110	–
1111	–	001	010	–	100	–	–	–

NOTE 1 – The error correction applied provides a DEDSEC (double error detection – single error correction) function. The received bits denoted by "–" in the table, if detected, indicate that an error has occurred but cannot be corrected.

2.4 Ancillary data

The ancillary signals should comply with the general rules of Recommendation ITU-R BT.1364.

2.5 Data words during blanking

The data words occurring during digital blanking intervals that are not used for the SAV, the EAV, the timing reference code ANC, or for ancillary data are filled with words corresponding to the following blanking levels, appropriately placed in the multiplexed data:

16.00 for *Y*, *R*, *G*, *B* signals

128.00 for C_B/C_R (time-multiplexed colour-difference signal).

3 Bit-parallel interface

For the 1125/60 system, the bits of the digital code words which describe the video signal are transmitted in parallel by means of 20 or 30 shielded conductor pairs. The 20 conductor pairs are used for the transmission of the signal set consisting of luminance *Y* and time-multiplexed colour-difference C_B/C_R components. The 30 conductor pairs are used for the transmission of *R*, *G*, *B* signals or *Y*, C_B/C_R components with an additional data stream (auxiliary channel). An additional shielded conductor pair carries the synchronous clock at 74.25 MHz.

For the 1250/50 system, the bits of the digital code words that describe the video signal are transmitted in parallel by means of 20 signal pairs, where each pair carries a stream of bits, 10 pairs for luminance data and 10 pairs for time-multiplexed colour-difference data. The 20 pairs can also carry ancillary data. A 21st pair provides a synchronous clock at 36 MHz (when sampling rate is 72 MHz), or at 27 MHz (when sampling rate is 54 MHz).

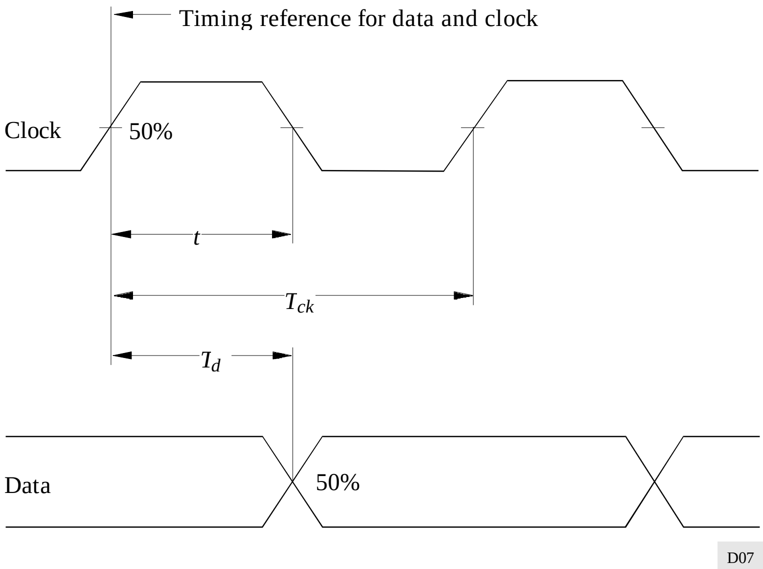
Data signals are transmitted in NRZ form in real time (unbuffered).

3.1 Clock signal and clock-to-data timing relationship

For 1125/60, the transmitted clock signal is a 74.25 MHz square wave, of which positive transitions occur midway between the data transitions as shown in Fig. 7 and Table 7.

FIGURE 7

Clock-to data timing relationship for 1125/60 (at sending end)



For 1250/50 at 72 MHz sampling rate, the transmitted clock signal is a 36 MHz square wave of unity mark/space ratio (27 MHz for 1250 at 54 MHz sampling rate), the transitions of which are coincident with the transition of the data (see Fig. 8). A logical high state of the clock is concurrent with *Y* and C_B data samples and a logical low state with *Y* and C_R data samples, as shown in Fig. 8 and Table 7.

TABLE 7

Clock signal specifications

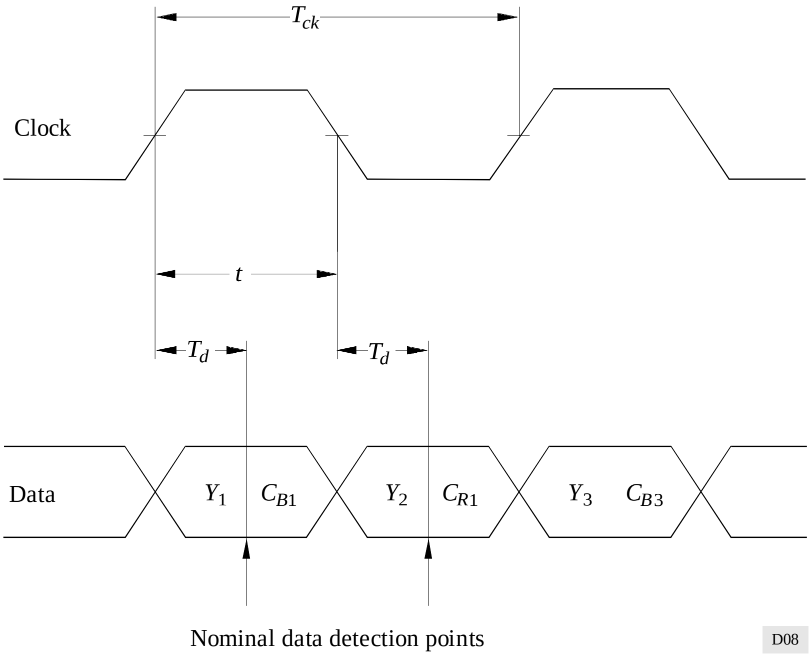
Parameter	Value			
	1125/60		1250/50	
Sampling frequency for *Y, R, G, B* signals	74.25 MHz	74.25/1.001 MHz	72 MHz	54 MHz
Clock period T_{ck} (ns)	1/(2200 f_H)		1/(1152 f_H)	1/(864 f_H)
	13.468 (nominal)	13.481 (nominal)	27.778 (nominal)	37.038 (nominal)
Clock pulse width *t* (ns)	6.734 ± 1.5	6.741 ± 1.5	13.889 (nominal)	18.519 (nominal)
Clock jitter	Within ± 0.5 ns from the average time of transition over one field			
Data timing T_d (ns)	6.734 ± 1.0	6.741 ± 1.0	6.944 (nominal)	9.259 (nominal)

NOTE 1 – f_H denotes the line frequency.

Values are specified at the sending end (source).

FIGURE 8

Clock to data timing relationship for 1250/50



3.2 Electrical characteristics of the interface

The interface employs 21 line drivers and line receivers, in the case of the transmission of Y and C_R/C_B components. Each line driver has a balanced output and the corresponding line receiver has a balanced input.

For 1125/60, the interface employs 31 line drivers and line receivers, in the case of R, G and B components or Y, C_R/C_B with an additional data stream (auxiliary channel). Although the use of ECL technology is not mandatory, the line driver and receiver must be ECL 10 kH compatible for 1125/60, and ECL 100 k compatible for 1250/50, i.e., they must permit the use of ECL for either drivers or receivers. The receiver must sense correctly the data when a random signal produces conditions represented by the eye diagram of Fig. 10.

TABLE 8

Line driver characteristics

Item	Parameter	Values	
		1125/60	1250/50
1	Output impedance (Ω)	110 maximum	100 maximum
2	Common mode voltage(1) (V)	–1.29 ± 15%	–1.3 ± 15%
3	Signal amplitude(2) (V)	0.6 to 2.0 p-p	0.8 to 2.0 p-p
4	Rise and fall times(3) (ns)	≤ 2.0	< 3
5	Difference between rise and fall times (ns)	≤ 1.0	

(1) Measured relative to ground.

(2) Measured across a resistive load having the nominal impedance of the assumed cables, that is 110 Ω for 1125/60 and 100 Ω for 1250/50.

(3) Measured between the 20% and 80% points across a resistive load having the nominal impedance of the assumed cable.

TABLE 9

Line receiver characteristics

Item	Parameter	Values	
		1125/60	1250/50
1	Input impedance (Ω)	110 ± 10	100 ± 10%
2	Maximum input signal voltage (V)	2.0 p-p	
3	Minimum input signal voltage (mV)	185 p-p	
4	Maximum common mode voltage(1) (V)	± 0.3	± 0.5
5	Differential delay(2) (ns)	4.0	4.5

(1) Comprising interference in the range DC to line frequency (fH).

(2) Data must be correctly sensed when the differential delay between the received clock and data is within this range.

FIGURE 9

Line driver and line receiver interconnection

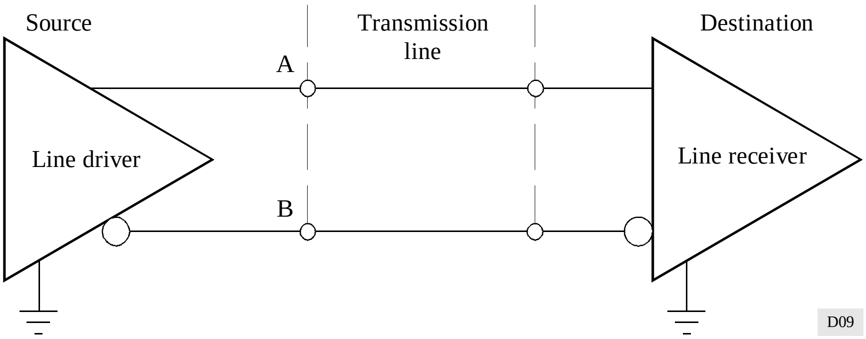
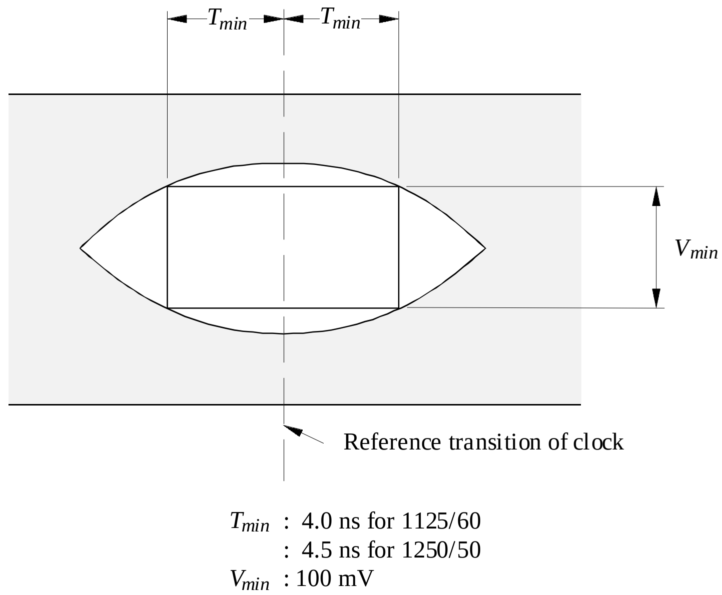


FIGURE 10

Idealized eye diagram corresponding to the minimum input signal level



Note 1 – For 1125/60, the width of the window in the eye diagram, within which data must be correctly detected, comprises ± 0.5 ns clock jitter, ± 1.0 ns data timing, and ± 2.5 ns propagation skew of conductor pairs.

For 1250/50, the aggregate of clock jitter, data timing and propagation skew of conductor pairs must not exceed 4.5 ns.

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3.3 Mechanical characteristics

3.3.1 Connector

The interface uses a multi-contact connector. Connectors are locked by two screws on the cable connectors and two threaded bolts on the equipment. Cable connectors employ pin contacts and equipment connectors employ socket contacts. Shielding of the connectors and cables is mandatory.

For 1125/60, a 93-contact connector is used. Contact assignments are indicated in Tables 10 and 11. The mechanical specifications for the connectors are shown in Figs. 11, 12 and 13.

For 1250/50, a 50-contact type D subminiature connector is used. Contact assignments are indicated in Table 12 and Fig. 14 (for information, suggested contact assignments for a CB header are shown in Fig. 15).

3.3.2 Interconnecting cable

For 1125/60, two types of multi-channel cable, either 21 or 31 channels, can be used in accordance with the transmission signal set (see Table 11). The cable consists of twisted pairs with individual shield of each pair. It also contains an overall shield. The nominal characteristic impedance of each twisted pair is 110 Ω. The cable shall provide the characteristics that satisfy the condition of eye diagram shown in Fig. 10 up to a maximum cable length of 20 m.

For 1250/50, 21-channel balanced conductor pairs is used. The nominal characteristic impedance of each conductor pair is 100 Ω. Cable length up to 30 m may be employed when a high-quality cable is used.

TABLE 10

Connector contact assignment for 1125/60 system

Contact	Signal line	Contact	Signal line	Contact	Signal line	Contact	Signal line	Contact	Signal line	Contact	Signal line
1	Clock A	17	GND	33	Clock B						
2	XD 9A	18	GND	34	XD 9B	49	YD 4A	64	GND	79	YD 4B
3	XD 8A	19	GND	35	XD 8B	50	YD 3A	65	GND	80	YD 3B
4	XD 7A	20	GND	36	XD 7B	51	YD 2A	66	GND	81	YD 2B
5	XD 6A	21	GND	37	XD 6B	52	YD 1A	67	GND	82	YD 1B
6	XD 5A	22	GND	38	XD 5B	53	YD 0A	68	GND	83	YD 0B
7	XD 4A	23	GND	39	XD 4B	54	ZD 9A	69	GND	84	ZD 9B
8	XD 3A	24	GND	40	XD 3B	55	ZD 8A	70	GND	85	ZD 8B
9	XD 2A	25	GND	41	XD 2B	56	ZD 7A	71	GND	86	ZD 7B
10	XD 1A	26	GND	42	XD 1B	57	ZD 6A	72	GND	87	ZD 6B
11	XD 0A	27	GND	43	XD 0B	58	ZD 5A	73	GND	88	ZD 5B
12	YD 9A	28	GND	44	YD 9B	59	ZD 4A	74	GND	89	ZD 4B
13	YD 8A	29	GND	45	YD 8B	60	ZD 3A	75	GND	90	ZD 3B
14	YD 7A	30	GND	46	YD 7B	61	ZD 2A	76	GND	91	ZD 2B
15	YD 6A	31	GND	47	YD 6B	62	ZD 1A	77	GND	92	ZD 1B
16	YD 5A	32	GND	48	YD 5B	63	ZD 0A	78	GND	93	ZD 0B

NOTE 1 – XD 9-XD 0, YD 9-YD 0, and ZD 9-ZD 0 represent each bit of the component signals. The suffix 9 to 0 indicates the bit number (bit 9 denotes MSB). A and B correspond to the terminals A and B of Fig. 9, respectively. The relationship between XD, YD, ZD and component signals are specified in Table 10.

NOTE 2 – The shield of each pair uses the ground contact (GND) located between A and B contacts for the signal, e.g., contact No. 17 is used for the shield of the clock signal. The overall shield of the cable is electrically connected to connector hood, which is grounded to the frame of the equipment.

TABLE 11

Transmission signal set and signal line assignment for 1125/60

Transmission signal set	Component	Signal line assignment		Cable
		10 bit system	8-bit system	
Y, C_R/C_B	Y	XD 9-XD 0	XD 9-XD 2	21 pairs
	C_R/C_B	ZD 9-ZD 0	ZD 9-ZD 2	
Y, C_R/C_B with auxiliary channel	Y	XD 9-XD 0	XD 9-XD 2	31 pairs
	C_R/C_B	ZD 9-ZD 0	ZD 9-ZD 2	
	Auxiliary channel	YD 9-YD 0	YD 9-YD 2	
R, G, B	G	XD 9-XD 0	XD 9-XD 2	
	B	YD 9-YD 0	YD 9-YD 2	
	R	ZD 9-ZD 0	ZD 9-ZD 2	

FIGURE 11

93-pin multi-pin connector (plug) for 1125/60

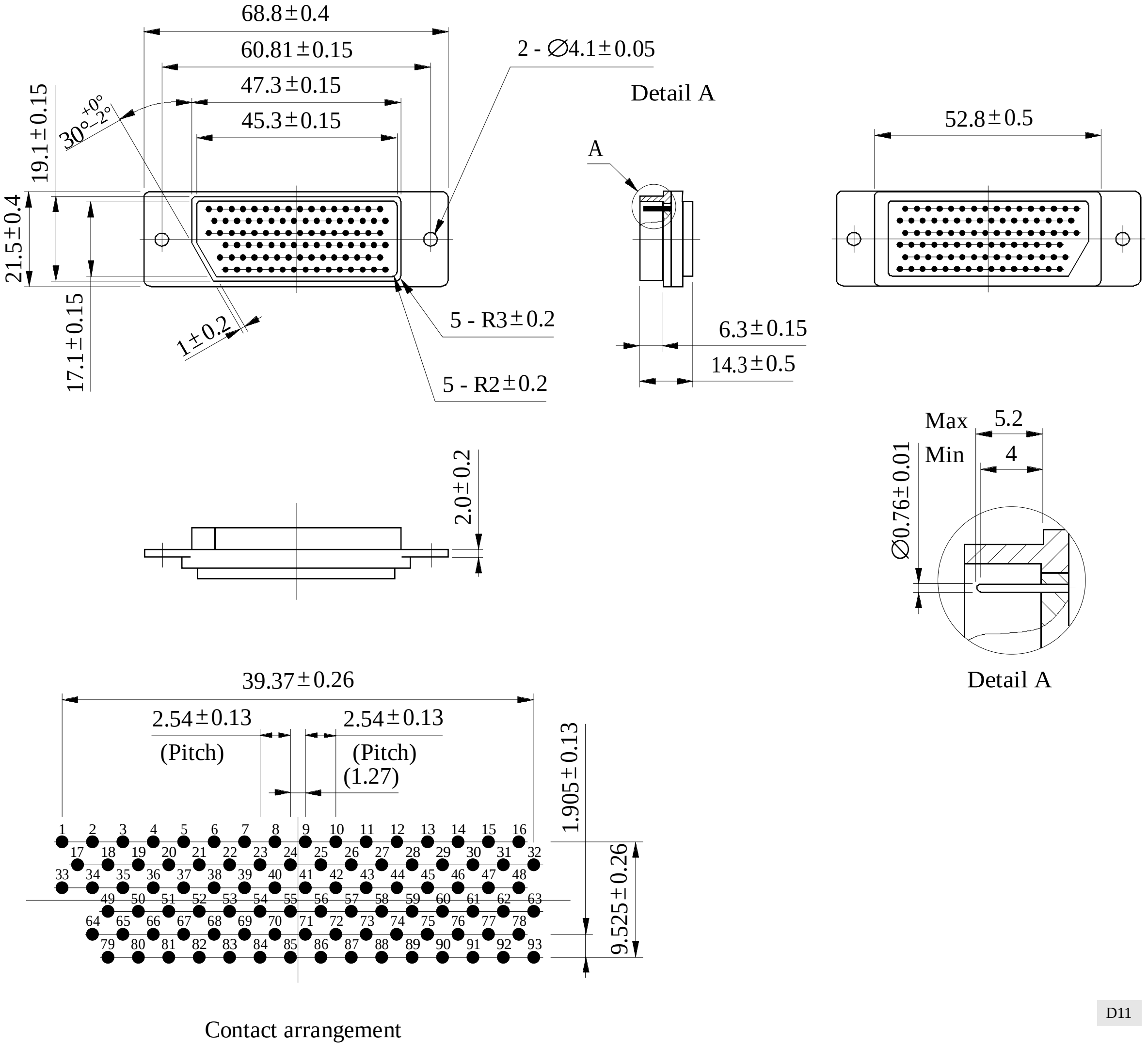


FIGURE 12

93-pin multi-pin connector (receptacle) for 1125/60

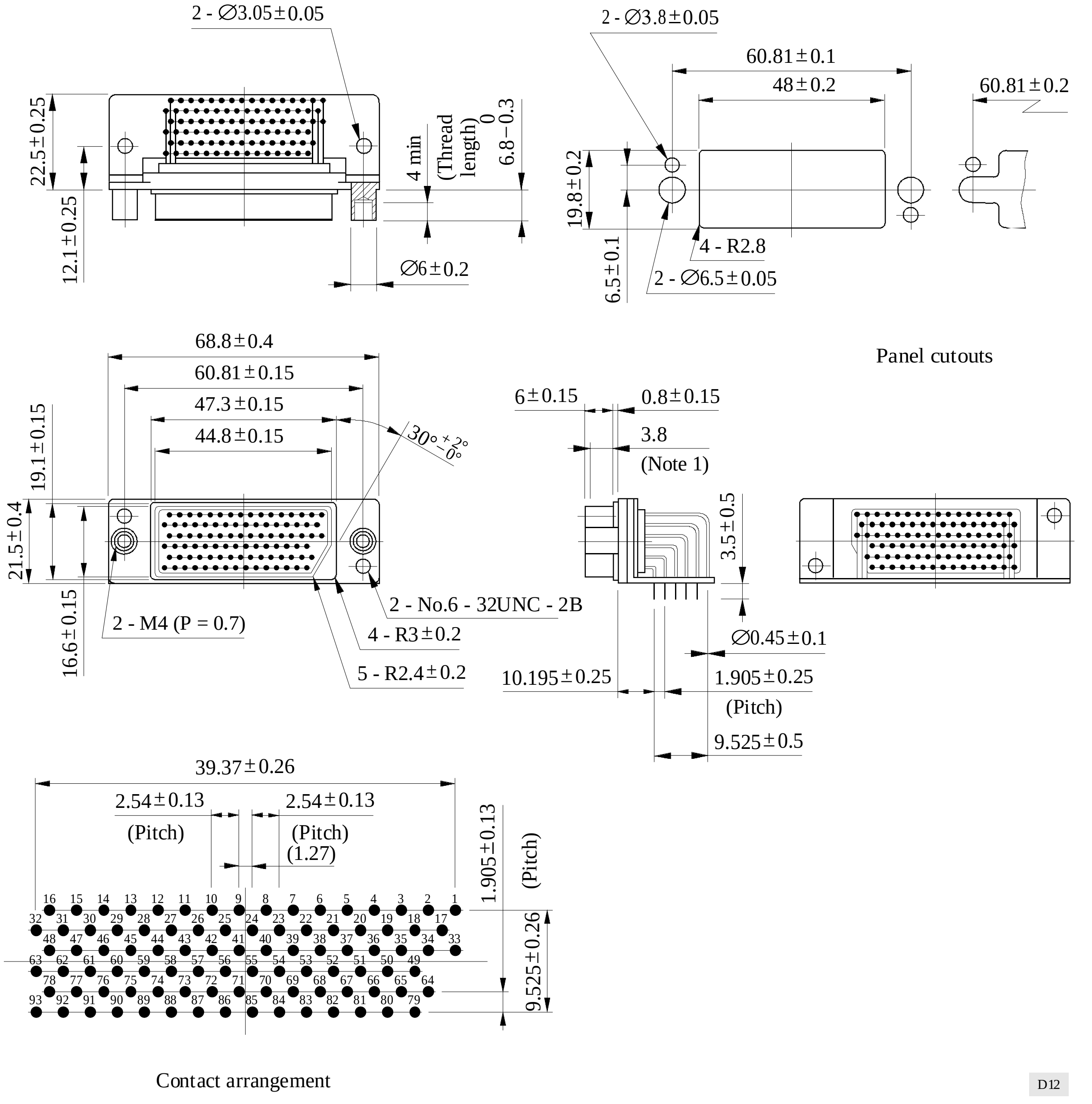
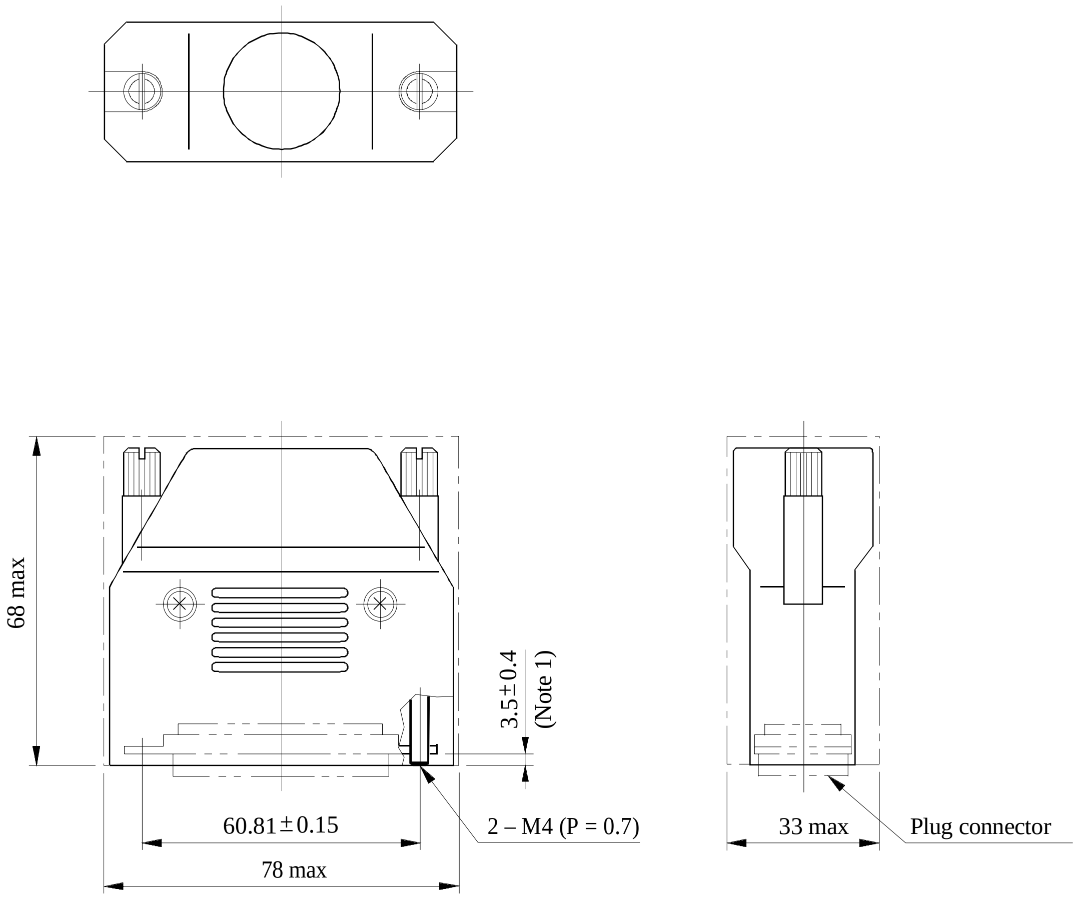


FIGURE 13

93-pin multi-pin connector (hood) for 1125/60



Note 1 – A screw projecting out from the plug connector.

Note 2 – Applicable outer diameter:
17.5 min to 19.3 max and 21.1 min to 23.2 max.

D13

TABLE 12

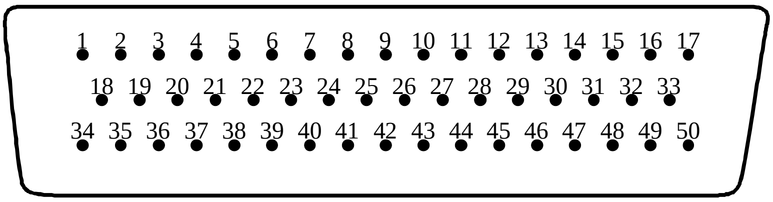
Connector contact assignment for 1250/50

Contact	Signal line	Contact	Signal line	Contact	Signal line
1	Clock A			34	Clock B
2	GND	18	GND	35	GND
3	Data 9A	19	GND	36	Data 9B
4	Data 8B	20	Data 8A	37	Data 7A
5	Data 6A	21	Data 7B	38	Data 6B
6	Data 5B	22	Data 5A	39	Data 4A
7	Data 3A	23	Data 4B	40	Data 3B
8	Data 2B	24	Data 2A	41	Data 1A
9	Data 0A	25	Data 1B	42	Data 0B
10	GND	26	GND	43	GND
11	Data 19A	27	GND	44	Data 19B
12	Data 18B	28	Data 18A	45	Data 17A
13	Data 16A	29	Data 17B	46	Data 16B
14	Data 15B	30	Data 15A	47	Data 14A
15	Data 13A	31	Data 14B	48	Data 13B
16	Data 12B	32	Data 12A	49	Data 11A
17	Data 10A	33	Data 11B	50	Data 10B

NOTE 1 – Data 9-Data 0 represent each bit of the luminance signal (Y), and Data 19-Data 10 that of time-multiplexed colour-difference signal (CR/CB). The suffix 19 to 0 indicates the bit number (bit 19 denotes MSB for CR/CB and bit 9 MSB for Y). A and B correspond to the terminals A and B of Fig. 9, respectively.

FIGURE 14

Mating face of connector receptacle containing male pins (plug) for 1250/50



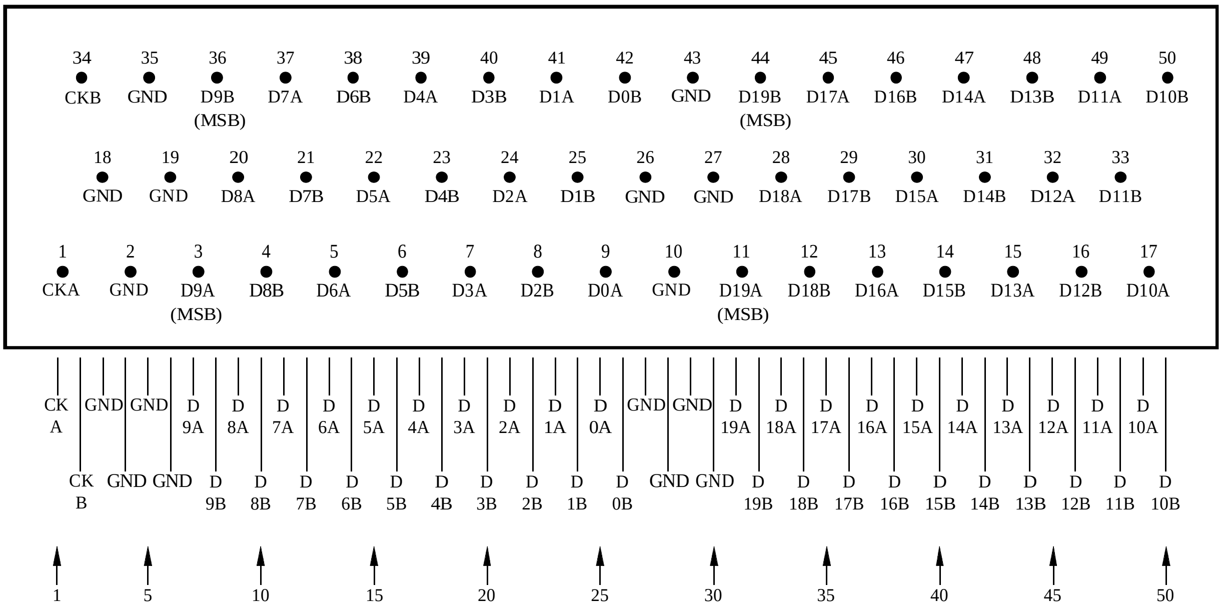
Note 1 – The preferred orientation for connectors, mounted vertically or horizontally, is with contact 1 uppermost.

D14

FIGURE 15

Suggested contact assignment for PCB header for 1250/50

50-way IDC (view looking at ID pins, pin numbers show corresponding 50-way D-type numbers)



50-way ribbon cable number

D15

4 Bit-serial interface

4.1 Data format

The bit-serial data consists of video data, video timing reference codes, line number data, error detection codes, ancillary data and blanking data. Each data has a word-length of 10 bits, and is represented as parallel data before serialization. Two parallel streams (i.e. luminance data Y and colour-difference data C_B/C_R) are multiplexed and serialized in accordance with § 4.2.

4.1.1 Video data

The video data should be 10-bit words representing Y, C_B/C_R of the video systems defined in § 1.

4.1.2 Video timing reference codes

The video timing reference codes, SAV and EAV have the same format as that defined in § 2.

4.1.3 Line number data

The line number data is composed of two words indicating the line number. The bit assignment of the line number data is shown in Table 13. The line number data should be located immediately after EAV.

TABLE 13

Bit assignment of the line number data

Word	b9 (MSB)	b8	b7	b6	b5	b4	b3	b2	b1	b0 (LSB)
LN0	not b8	L6	L5	L4	L3	L2	L1	L0	R	R
LN1	not b8	R	R	R	L10	L9	L8	L7	R	R

L0 (LSB)-L10 (MSB): line number in binary code

R: reserved (set to zero)

4.1.4 Error detection codes

The error detection codes CRCC (cyclic redundancy check codes), which are used to detect errors in active digital line, EAV and line number data, consist of two words and are determined by the following polynomial generator equation:

$$EDC(x) = x^{18}+x^{5}+x^{4}+1$$

Initial value of the codes is set to zero. The calculation starts at the first word of the digital active line and ends at the final word of the line number data. Two error detection codes are calculated, one for luminance data, *YCR*, and one for colour-difference data, *CCR*. The bit assignment of the error detection codes is shown in Table 14. The error detection codes should be located immediately after the line number data.

4.1.5 Ancillary data

The ancillary data should comply with general rules of Recommendation ITU-R BT.1364.

4.1.6 Blanking data

The blanking data words during digital blanking intervals that are not used for SAV, EAV, the line number data, the error detection codes and the ancillary data, should be filled with the words corresponding to the following quantization levels:

16.00 for Y data

128.00 for C_B/C_R data

TABLE 14

Bit assignment for error detection codes

Word	b9 (MSB)	b8	b7	b6	b5	b4	b3	b2	b1	b0 (LSB)
YCR0	not b8	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
YCR1	not b8	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9
CCR0	not b8	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
CCR1	not b8	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9

NOTE 1 – CRC0 is the MSB of error detection codes

4.2 Transmission format

The two parallel data streams are transmitted over a single channel in bit-serial form after word-multiplexing, parallel-to-serial conversion and scrambling.

4.2.1 Word-multiplexing

The two parallel streams should be multiplexed word by word into a single 10-bit parallel stream in the order of C_B, Y, C_R, Y, C_B, Y, C_R, Y..........(See Fig. 16)

4.2.2 Serializing

The least significant bit (LSB) of each 10-bit word in the word-multiplexed parallel stream should be transmitted first in the bit-serial format.

4.2.3 Channel coding

The channel coding scheme should be scrambled NRZI (non-return to zero inverted). The serialized bit stream should be scrambled using the following generator polynomial equation:

$$G(x) = (x^9+x^4+1)(x+1)$$

The input signal to the scrambler shall be positive logic. (The high voltage represents data 1 and the lowest voltage represents data 0.)

4.3 Coaxial cable interfaces

The coaxial cable interfaces consists of one source and one destination in a point-to-point connection. The coaxial cable interfaces specify the characteristics of line driver (source), line receiver (destination), transmission line and connectors.

4.3.1 Line driver characteristics (source)

Table 15 specifies the line driver characteristics. The line driver should have an unbalanced output circuit.

4.3.2 Line receiver characteristics (destination)

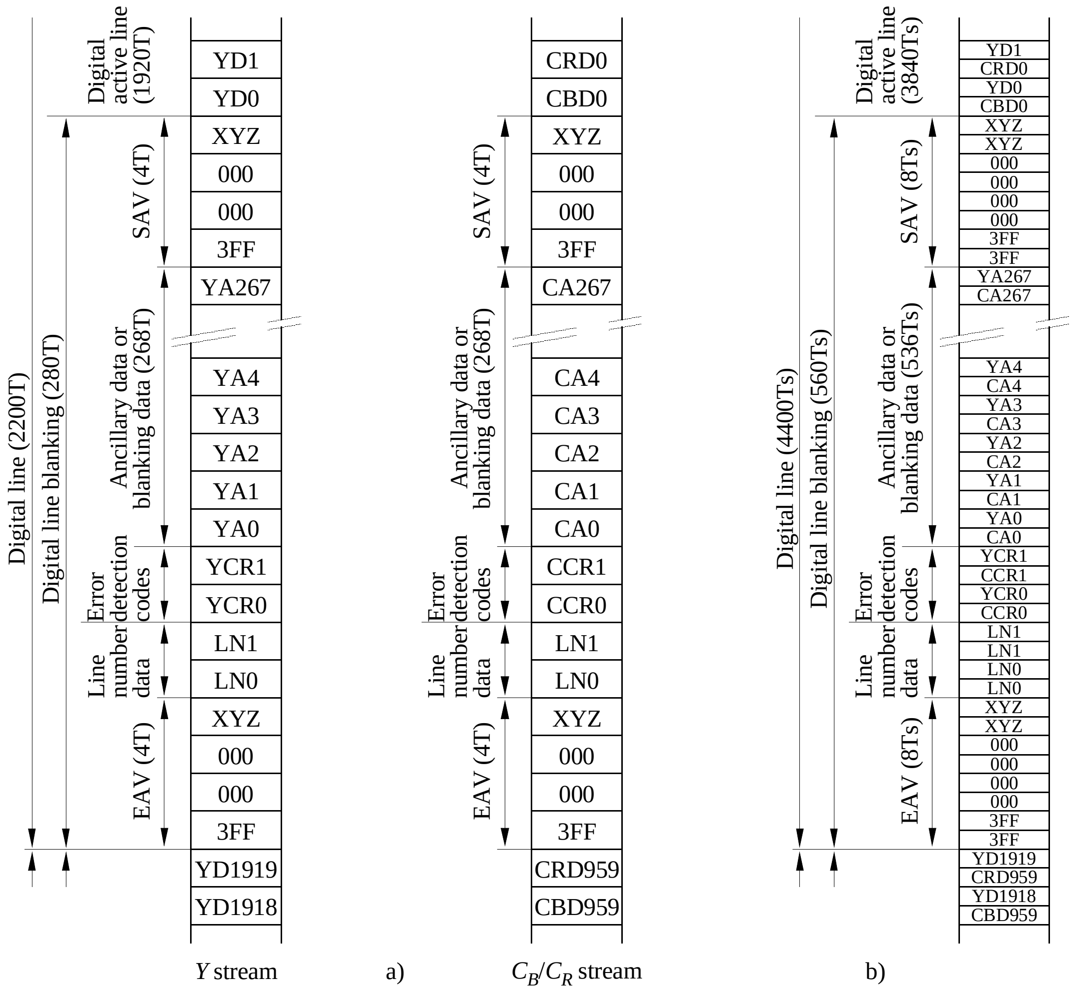
Table 16 specifies the line receiver characteristics. The line receiver should have an unbalanced input circuit. It must sense correctly the received data when connected to a line driver operating at the extreme voltage limits permitted by § 4.3.1, and when connected through a cable having the worst condition permitted by § 4.3.3.

4.3.3 Transmission line characteristics

Relevant specifications are given in Table 17.

FIGURE 16

Data stream for 1125/60 signal



a) Parallel data streams *Y* and C_B/C_R

b) Multiplexed parallel data stream

The LSB of each word should be transmitted first when it is transmitted as bit-serial data

YD0 - YD1919	Digital luminance data *Y*
CBD0 - CBD959	Digital colour-difference data C_B
CRD0 - CRD959	Digital colour difference data C_R
YA0 - YA267	Ancillary data or blanking data in Y stream
CA0 - CA267	Ancillary data or blanking data in C_B/C_R stream
T:	1/74.25 MHz = 13.468 ns or 1.001/74.25 MHz = 13.481 ns

$T_S = T/2$

1120-16

TABLE 15

Line driver characteristics

Item	Parameter	Value
1	Output impedance	75 Ω nominal
2	DC offset [(1)]	0.0 V ± 0.5 V
3	Signal amplitude [(2)]	800 mV_{p-p} ± 10%
4	Return loss	≥15 dB [(3)], ≥10 dB [(4)]
5	Rise and fall times [(5)]	<270 ps (20% to 80%)
6	Difference between rise and fall time	≤ 100 ps
7	Output jitter [(6)]	f_1 = 10 Hz f_3 = 100 kHz f_4 = 1/10 of the clock rate A_1 = 1 UI (UI; unit interval) A_2 = 0.2 UI

(1) Defined by mid-amplitude point of the signal.

(2) Measured across a 75Ω resistive load connected through a 1 meter coaxial cable.

(3) In the frequency range of 5 MHz to 742.5 MHz.

(4) In the frequency range of 742.5 MHz to 1.485 GHz.

(5) Determined between the 20% and 80% amplitude points and measured across a 75 Ω resistive load. Overshoot of the rising and falling edges of the waveform shall not exceed 10% of the amplitude.

(6) For 1125/60 system, 1 UI and 0.2 UI correspond to 673 ps and 135 ps, respectively. For 1250/50 system, 1 UI and 0.2 UI correspond to 694 ps (72 MHz sampling), 926 ps (54 MHz sampling) and 139 ps (72 MHz sampling), 185 ps (54 MHz sampling), respectively. Specification of jitter and jitter measurements methods shall comply with Recommendation ITU-R BT.1363 (Jitter specifications and jitter measurement methods of bit-serial signals conforming to Recommendation ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120).

Output amplitude excursions due to signals with a significant dc component occurring for a horizontal line (pathological signals) shall not exceed 50 mV above or below the average peak-peak signal envelope. (In effect, this specification defines a minimum output coupling time constant.)

TABLE 16

Line receiver characteristics

Item	Parameter	Value	
1	Input impedance	75 Ω nominal	
2	Return loss	≥15 dB [(1)], ≥10 dB [(2)]	
3	Interfering signal	± 2.5 V_{max}	DC
		< 2.5 V_{p-p}	below 5 kHz
		< 100 mV_{p-p}	5 kHz to 27 MHz
		< 40 mV_{p-p}	above 27 MHz
4	Input jitter [(3)]	to be defined	

(1) In the frequency range of 5 MHz to 742.5 MHz.

(2) In the frequency range of 742.5 MHz to 1.485 GHz.

(3) Specification of jitter and jitter measurements methods shall comply with Recommendation ITU-R BT.1363 (Jitter specifications and jitter measurement methods of bit-serial signals conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120).

Values for input jitter need to be defined. Input jitter is measured with a short cable (2 m).

TABLE 17

Transmission line characteristics

Item	Parameter	Value
1	Transmission loss [(1)]	≤ 20 dB at 1/2 clock frequency
2	Return loss	≥15 dB [(2)], ≥10 dB [(3)]
3	Impedance	75 Ω nominal

(1) Loss characteristics of $1/\sqrt{f}$.

(2) In the frequency range of 5 MHz to 742.5 MHz.

(3) In the frequency range of 742.5 MHz to 1.485 GHz.

4.3.4 Connector

The connector should have the mechanical characteristics conforming to the standard BNC type defined in IEC 169-8, and its electronic characteristics should provide for a characteristic impedance of 75 Ω and for a usable frequency range of up to 2.4 GHz.

4.4 Optical fibre interfaces

Optical interfaces should use single mode optical interfaces only and should comply with general rules of Recommendation ITU-R BT.1367 (Serial Digital Fiber Transmission Systems for Signals Conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120).

To make use of this Recommendation the following specifications are necessary:

Rise and fall times < 270 ps (20% to 80%)

output jitter (See Note 1)
f_1 = 10 Hz
f_3 = 100 kHz
f_4 = 1/10 of the clock rate
A_1 = 0.135 UI (UI; unit interval)
A_2 = 0.135 UI

Input jitter needs to be defined. Input jitter is measured with a short cable (2 m).

NOTE 1 – Specification of jitter and jitter measurements methods shall comply with Recommendation ITU-R BT.1363 (Jitter specifications and jitter measurement methods of bit-serial signals conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120).